KSZ8462HL Evaluation Board User Guide

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Introduction

The KSZ8462HL Evaluation Board provides a platform in which to test or explore the functionally of the KSZ8462HL IEEE 1588 Precision Time Protocol (PTP) enabled switch products.

The KSZ8462HL and KSZ8462FHL devices are highly integrated 2-port 10BASE-T / 100BASE-TX/FX managed Ethernet switches with generic parallel host interface connectivity to a host on Port 3. This is the ideal solution in industrial applications where real time clock synchronization using Ethernet connectivity across a network is desired. The KSZ8462HL includes all the functions of a 10/100BASE-T/TX/FX switch system that combines switch engine, frame buffers management, addresses look-up table, queue management, MIB counters, media access controllers (MAC) and PHY transceiver interfaces. The KSZ8462HL is fully compliant with the IEEE 1588 (Version 2) Precision Time Protocol and IEEE 802.3 standards (10BASE-T and 100BASE-TX/FX).

This KSZ8462HL Evaluation Board User Guide provides the information necessary to configure and set up the board to evaluate or test the KSZ8462HL devices in different environments.

1 Board Features

The KSZ8462HL Evaluation Board encompasses the following features.

- Micrel's KSZ8462HL Integrated 3-Port 10/100 Managed Ethernet Switch
- Fully compatible with the KSZ8462FHL
- Two Ethernet LAN Interfaces with RJ-45 jacks and isolation magnetics (Port 1 & 2)
- Auto MDI/MDI-X for automatic detection and correction for straight-through and crossover cables
- Generic 8/16 bit parallel Host processor interface (Port 3)
- Provisioning for two 100BASE-FX fiber interfaces (optional)
- Provisioning for line side and chip side over-voltage protection (optional)
- On-board 3.3V and 1.8V/2.5V regulators
- Configurable for VDDIO of 3.3V, 2.5V, or 1.8V operation
- Serial port interface for EEPROM
- LED indicators for link status and activity of the RJ-45 ports
- On-board 25 MHz crystal
- Jumpers for power up configuration of the device
- Jumpers for GPIO pins, I/O voltage selection and serial-port connections
- 5V DC voltage required for operation
- Reset switch
- Various test points

2 KSZ8462HL Evaluation Board Kit

The KSZ8462HL Evaluation Board kit includes the following:

- KSZ8462HL Evaluation Board
- KSZ8462HL Evaluation Board User's Guide (This document, available in the eval kit, on the Micrel website)
- KSZ8462HL Evaluation Board Schematic (Available in the eval kit, on the Micrel website)

3 Hardware Description

The KSZ8462HL Evaluation board is a small form-factor board (5.2” x 4.75”) that can be configured by a host processor connected through the 16-bit generic parallel host interface. In addition to passing full-rate Ethernet traffic, the external host processor can read and write the entire register set within the KSZ8462 device through this interface.

The board supports different types of host processors. Therefore a strap-in configuration mode is provided to set the parallel interface according to the type of processor used. Strap-in mode configuration occurs at power on time where the voltage level on certain pins is automatically sampled and used to configure various features in the device. This is accomplished with the on board jumper options.

Available configuration options are explained in detail in the following sections. Figure 1 is a picture of the KSZ8462HL Evaluation board.

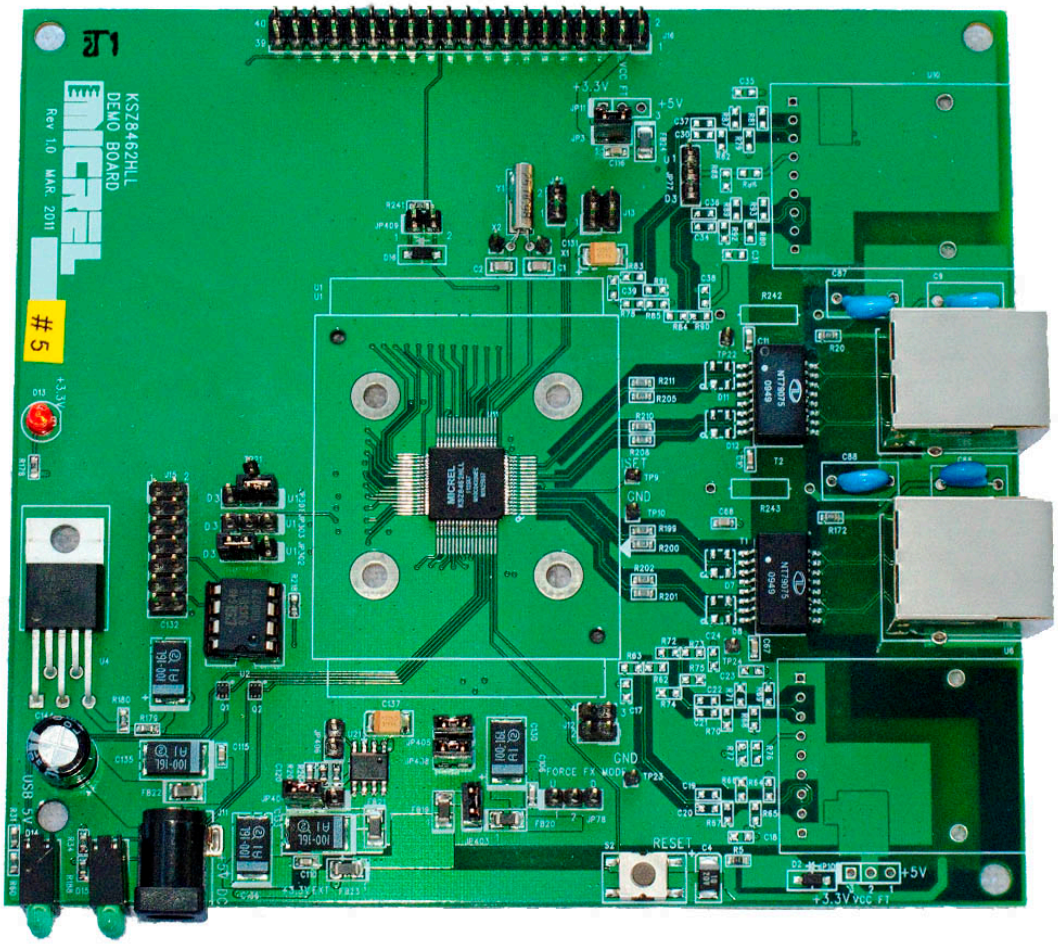

Figure 1 KSZ8462HL Evaluation Board

3.1 Device Configuration

3.1.1 Strap-in Configuration

Strap-in configuration is used for setting up the parallel host interface and to indicate the presence of an EEPROM. This is accomplished by setting available configuration jumpers which are used at device power-up. Simply set the board's configuration jumpers to the desired settings and apply power to the board. The configuration can be changed while power is applied to the board by changing the jumper settings and pressing the convenient manual reset button for the new settings to take effect. Note that even if no external strap-in jumpers are set, internal pull-up and pull-down resistors will set the KSZ8462 to the default configuration.

The following table covers each jumper used for the strap-in option and describes its function.

JUMPER	FUNCTION	SETTING	DEFAULT
JP301	Parallel Bus Width select	Pins 1-2 closed: 16-bit Pins 2-3 closed: 8-bit	16-bit
JP302	Parallel Bus Endian-mode select	Pins 1-2 closed: Little Endian Pins 2-3 closed: Big Endian	Little Endian
JP303	EEPROM select	Pins 1-2 closed: EEPROM present Pins 2-3 closed: EEPROM not present	EEPROM not present

Table 1 Strap-In Configuration Jumpers

3.1.2 EEPROM Configuration

The KSZ8462HL Evaluation Board has a serial EEPROM to enable loading the MAC address into the device at power-up time with a pre-programmed value. The strap-in option should be set to enable the EEPROM presence, as indicated on the above table. If enabled, the first seven words of the Serial EEPROM will be read. Registers 0x010 – 0x015 will be loaded with words 0x01 – 0x03 from the EEPROM.

In addition, the remainder of EEPROM space (0x07 – 0x3F) can be written or read and used as needed by the host processor.

Supported EEPROM: 93C46

3.2 Power Supplies

The board requires a single 5V DC supply, which can be provided through a barrel power-supply jack (J11) or through the parallel host port. The current requirement is 200mA. When configured for fiber operation, expect the fiber modules to draw approximately 250mA of additional current per port.

The pin diameter of jack J11 is 2.5mm on early boards, and is 2.1mm on newer boards. 2.5mm plugs are recommended because they are generally compatible with both jack sizes. A 2.1mm plug, however, cannot be used with the 2.5mm jack.

JP3 must be in place if the board is powered through the parallel port. There is a 3.3V regulator on the board supplying power for the KSZ8462 and other components. A separate on-board voltage regulator is

provided for the optional 2.5V and 1.8V supplies for KSZ8462's I/O interface (VDD_IO). JP404 and JP406 are used for VDD_IO selection. JP403 and JP405 must be in place and other options properly selected before powering up the board.

JUMPER	FUNCTION	SETTING		
JP3	Enable +5V supply from host-port connector J16	Closed: enabled Open: disabled, use external power supply through J11		
JP403	+3.3V supply for KSZ8462 analog circuits	Must be closed		
JP405	+1.2V supply for KSZ8462 analog circuits	Must be closed		
JP408	+1.2V supply for KSZ8462 digital circuits	Must be closed		
	VDD_IO selection	**3.3V**	**2.5V**	**1.8V**
JP404		Pins 2-3 closed	Pins 1-2 closed	Pins 1-2 closed
JP406		X	open	Closed

Table 2 Power Supply Related Jumpers

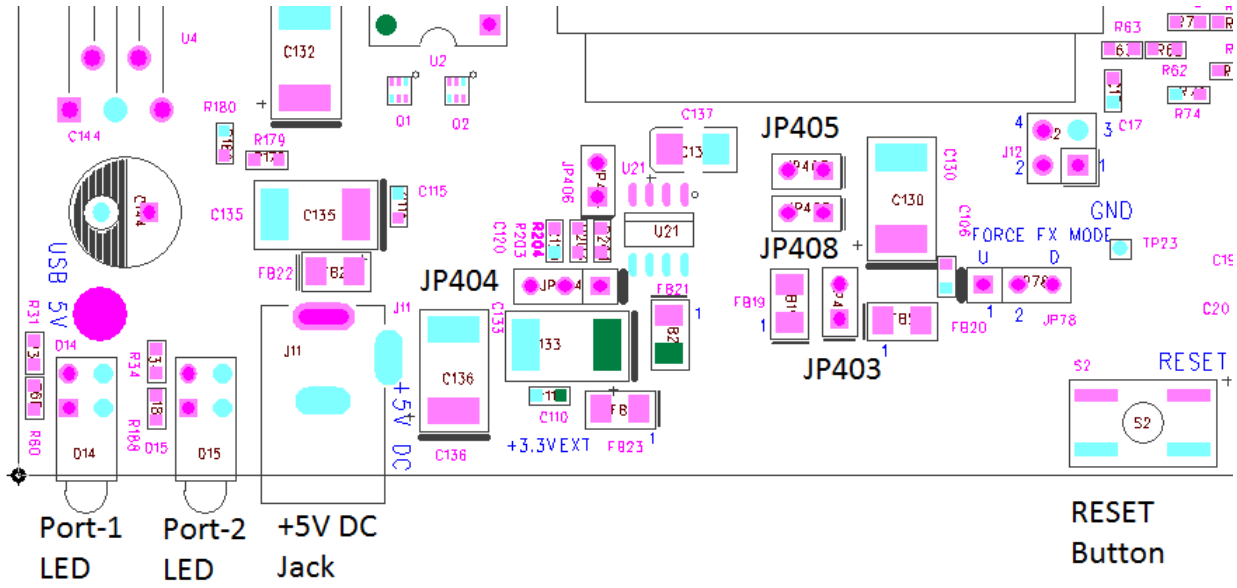

Figure 2 Power Supply Section and Related Jumper Locations

3.3 Port 3 Parallel Host Interface

The board features a 40-pin connector (J16) for interfacing the Bus Interface Unit (BIU) on the KSZ8462HL to an external host processor. The BIU is a generic parallel host interface providing access to the MAC of Port 3.

The 40-pin connector is a standard dual-row straight pin header. In order to evaluate the IEEE1588 PTP functionality, a host processor board such as the Micrel KSZ9692MII-PTP-EV or KSZ9692PB-PTP-EVAL board has to be connected to the parallel interface. Strap-in configurations determine the mode of host interface operation at power-up.

The voltage level on all interface pins (VDD_IO) can be set to 1.8V, 2.5V or 3.3V of operation, enabling a direct connection to different type of host processors.

Signal	Pin No.	Type	Function
SD[15:0]	5-20	I/O	**Shared Data Bus** In **16-bit** mode: SD[15:0] -> D[15:0] data access when CMD = "0". SD[10:2] -> A[10:2] address access and SD[15:12] -> BE[3:0] byte enable access when CMD = "1" (SD[1:0] and SD[11] are not used). In **8-bit** mode: SD[7:0] -> D[7:0] data access when CMD = "0". SD[7:0] -> A[7:0] 1st address access and SD[2:0] -> A[10:8] 2nd address access when CMD = "1" (SD[7:3] are not used during 2nd address access).
CMD	28	Input	**Command Type** This command input determines the SD[15:0] shared data bus access cycle information. 0: Data access 1: Command access for address and byte enable
CSN	23	Input	**Chip Select Enable** Chip Enable is an active low signal used to enable the shared data bus access.
INTRN	31	Output	**Interrupt** This low active signal asserted low when an interrupt is being requested.
RDN	36	Input	**Asynchronous Read** This low active signal is asserted to low during a read cycle. A 4.7K pull-up resistor is recommended on this signal.
WRN	35	Input	**Asynchronous Write** This low active signal is asserted low during a write cycle.
PME/ EEPROM	27	Output/ Input	**Power Management Event** This output signal indicates that a Wake On LAN event has been detected. The KSZ8462HL is requesting the system to wake up from low power mode. Its assertion polarity is programmable with the default polarity to be active low. **EEPROM select Configuration Mode** During Power-on/Reset time this pin is an input and the strap-in value is read by KSZ8462HL to determine the presence of an EEPROM. (see description of JP303 in Table 1)
RSTN	24	Input	**Reset** This is the Hardware reset pin. It is active Low. This reset input is required to be low for a minimum of 10 ms after supply voltages VDD_IO and 3.3V are stable.
+5V	1, 3		**Power supply** Connection to +5V supply of the Host processor board.
GND	2, 4, 21, 22, 25, 26, 29, 33, 34, 37-40		**Ground**
N.C.	30, 32		

Table 3 Signal Descriptions on the Parallel (Host-Port) Connector J16

3.4 GPIO pins

KSZ8462HL chip has up to 7 General Purpose I/O (GPIO) pins which are available on the evaluation board at connector J15. Three GPIO pins of the KSZ8462HL device are shared with EEPROM signals and are user programmable. By default the EEPROM signals are enabled, therefore initially only 4 GPIO pins are available. If more than 4 GPIO pins are required, the user needs to program IOMXSEL register (0x0D6) as follows:

IOMXSEL register (0x0D6)	Description	Setting
Bit 5	Selection of EESK or GPIO3 for Pin 53	1 = This pin is used for EESK (default) 0 = This pin is used for GPIO3
Bit 2	Selection of EEDIO or GPIO4 for Pin 54	1 = This pin is used for EEDIO (default) 0 = This pin is used for GPIO4
Bit 1	Selection of EECS or GPIO5 for Pin 55	1 = This pin is used for EECS (default) 0 = This pin is used for GPIO5

Table 4 GPIO Pin Selection for KSZ8462HL

GPIO signals are on the odd numbered pins of connector J15. All even numbered pins are GND connections. The GPIO pins can be used for any general purpose I/O as well as to support IEEE1588 PTP functionality.

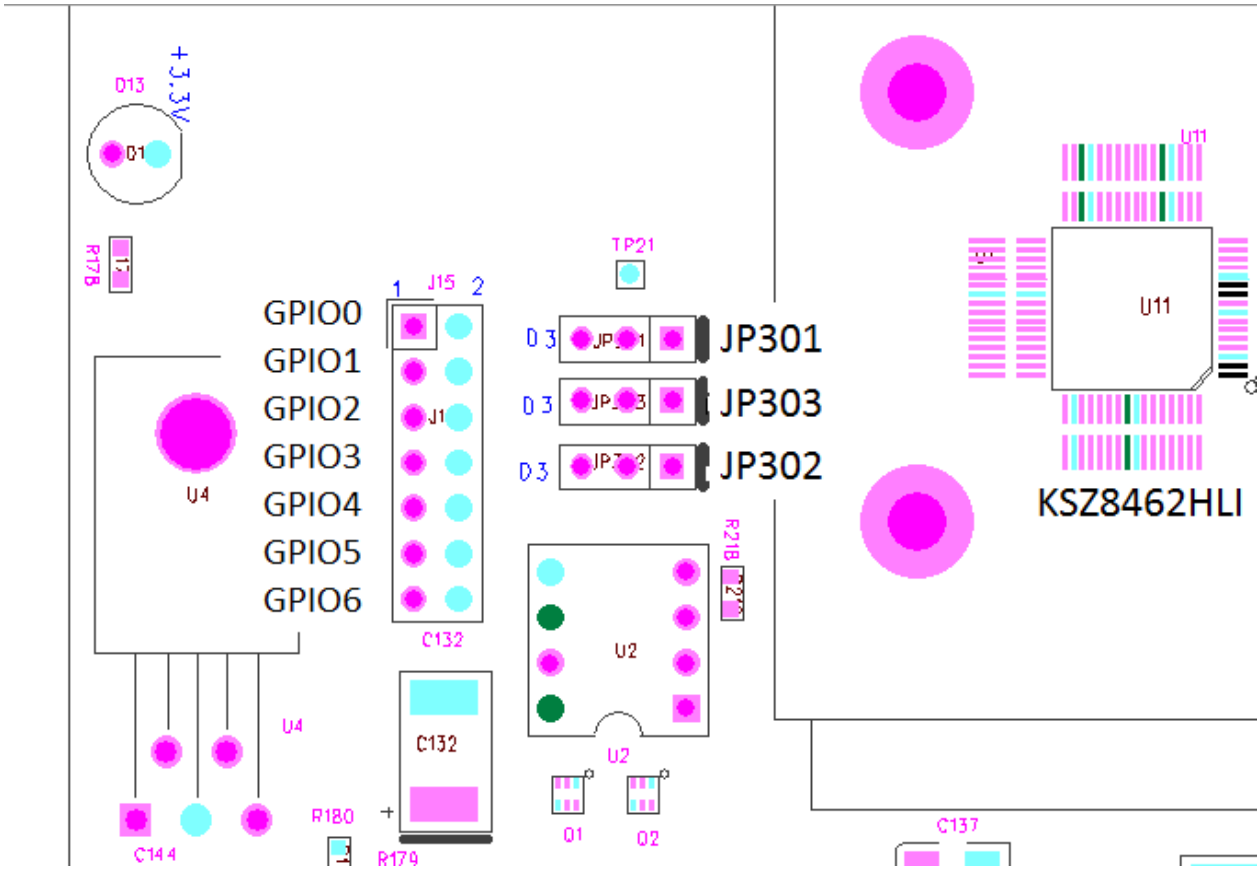

Figure 3 GPIO Connectors and Strap-in Jumper Locations

3.5 10/100 Ethernet PHY Ports

There are two 10/100 Ethernet PHY ports on the KSZ8462HL evaluation board. The ports can be connected to an Ethernet traffic generator or analyzer via standard RJ-45 connectors using CAT-5 (or better) UTP cables. Both ports support auto MDI/MDI-X, eliminating the need for cross-over cables.

Transformers are utilized for proper interfacing to an Ethernet network. In addition, optional over- voltage protection devices D5 thru D12 may be installed to protect the KSZ8462 in the event of an over- voltage condition.

For 10/100 Ethernet, the FXSD1 and FXSD2 pins should be pulled low by installing jumpers on pins 3 & 4 of J12 and J13.

3.6 100BASE-FX Fiber Port Option

There are two 100BASE-FX PHY ports on the KSZ8462HL evaluation board, which are not populated with necessary components. The ports can be connected to an Ethernet traffic generator or analyzer via fiber transceiver and fiber cable. In 100BASE-FX operation, both fiber signal detect input FXSD1 and FXSD2 are usually connected to the fiber transceiver SD (signal detect) output pin. This is done by jumpering pins 1 & 2 of J12 (Port 1) and J13 (Port 2). No jumpers are required on JP77 and JP78 except as noted below. Capacitors C5 and C6 are also generally not required.

100BASE-FX is supported by the KSZ8462FHL. All KSZ8462 devices power up in copper mode. Fiber Mode is selected by clearing the appropriate bits in the GFCR register (0x0D8 – 0x0D9).

The fiber signal detect threshold is set to 1.7V internally, When FXSD is less than the threshold, no fiber signal is detected and a far-end fault (FEF) is generated. When FXSD is over the threshold, the fiber signal is detected. To ensure proper operation, a resistive voltage divider is recommended to adjust the fiber transceiver SD output voltage swing to match the FXSD pin's input voltage threshold.

Alternatively, the user may choose not to implement the FEF feature. In this case, the FXSD input pin may be pulled high via jumpers JP77 and JP78.

3.7 LED Indicators

The KSZ8462HL evaluation board provides two LEDs (PxLED1, PxLED0) for each PHY port. The LED indicators are programmable to four different states. LED mode is selected through bits [9:8] of the SGCR7 register (0x00E-0x00F).

The LED mode definitions are specified in Table 7. See Figure 2 for the LEDs' orientation on the KSZ8462HL evaluation board in the power supply section.

SGCR7 Control Register (0x00E-0x00F) Bits[9:8]			
00 (default)	**01**	**10**	**11**
PxLED1 = Speed	PxLED1 = Active	PxLED1 = Duplex	PxLED1 = Duplex
PxLED0 = Link/Active	PxLED0 = Link	PxLED0 = Link/Active	PxLED0 = Link

Table 5 LED Functions

The KSZ8462HL evaluation board also has a power LED (D3) for the 3.3V power supply. When D3 is illuminated, the board's 3.3V power supply is "on".

The activity LED indicators for Port-1 and Port-2 are powered by 3.3V, regardless of the VDD_IO selected for the device.

3.8 List of Jumpers and Connectors

Jumper	Description	Setting
JP2	PWRDN Chip Power-down	Place Jumper for full chip power-down
JP3	Enable +5V supply from host-port connector	Closed: enabled Open: disabled
JP10, 11	Power selection for the Fiber module	Leave open when no Fiber Module present
JP77, 78	FXSD1, FXSD2 Fiber signal detect input for Port 1 and Port 2 (not used)	
JP301-303	Strapping options	See Table 1
JP403-408	Power-supply strapping options	See Table 2
JP409	Enable bi-directional Reset signal	Closed: enable Reset signal on both directions Open: Local reset signal does not affect the host processor board.
J1, J2	RJ45 connectors for Port-1 and Port-2	
J11	+5V DC Power Jack	
J12, J13	FXSD pin connections	Pins 1-2 closed: connect to SD signal from fiber module Pins 3-4 closed: ground the FXSD pins, for copper mode
J15	GPIO Header	
J16	Parallel Host-port interface (Port-3)	

Table 6 List of Jumpers and Connectors

3.9 Board Layout

The layout of the board is shown in Figure 3. The key areas are indicated.

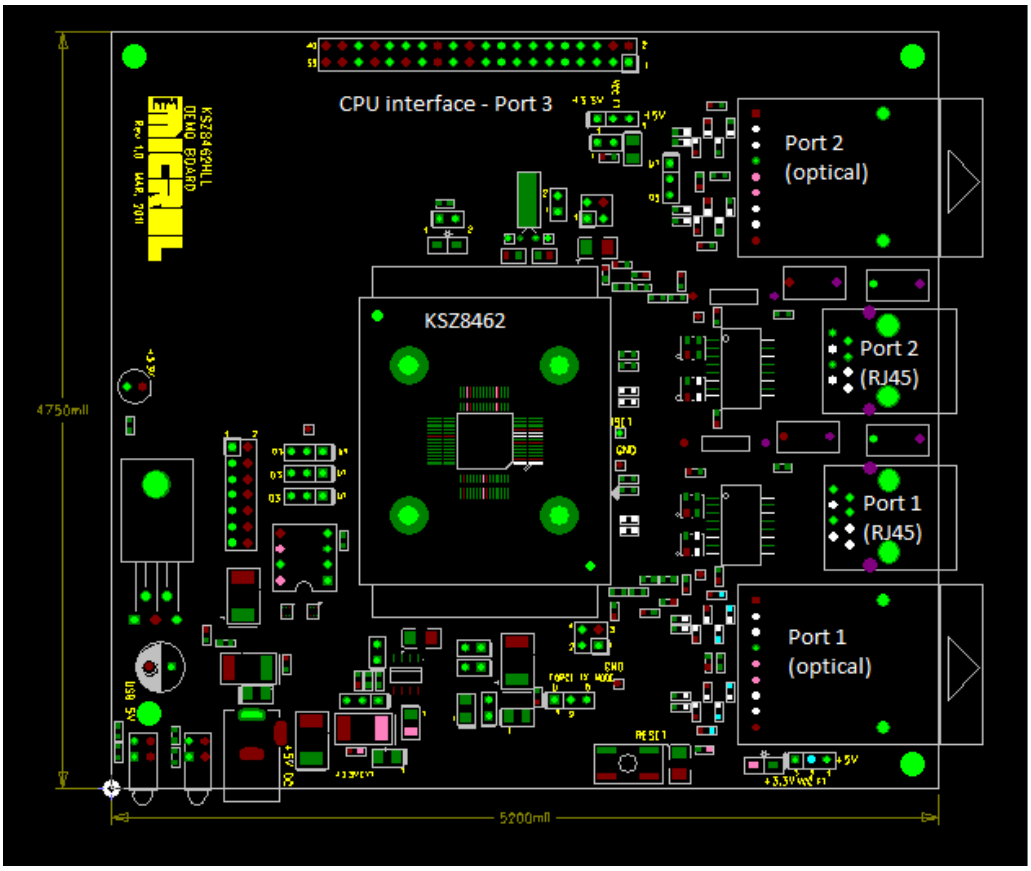

Figure 4 Topside Layout of the Board

The KSZ8462HL Evaluation board, together with the KSZ9692PB SOC board (KSZ9692-MII-PTP-EV), provides a complete evaluation platform for the IEEE1588 PTP functionality. In this setup, Port3 of the KSZ8462 evaluation board is connected to the SOC board through its parallel host interface. For more details on this configuration, refer to the KSZ8462HL Evaluation Kit User Guide.

4 Using the KSZ8462HL Evaluation Board

The Evaluation Board is intended to provide a platform that enables designers to investigate and evaluate the capabilities of the KSZ8462 device. It is not intended to be a complete development system to be used for an entire product design effort.

5 Reference Documents

KSZ8462HL Datasheet (Contact Micrel for latest Datasheet)
KSZ8462HL Evaluation Board Schematic (Contact Micrel for latest Schematic)
KSZ8462HL Evaluation Board Gerber files
IEEE802.3 Specification
KSZ8462HL Evaluation Kit User Guide

6 Revision History

Revision	Date	Summary of Changes
0.1	9/30/2011	- Initial Release - Updated Table 4 for Pin #'s. - Replaced 8463 with 8462.
1.0	7/17/2013	- Replace HLI with HL - General update