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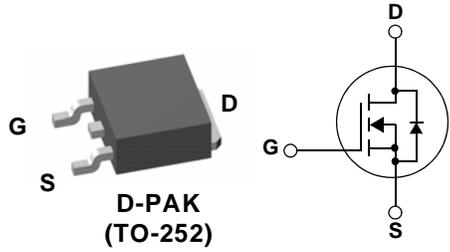
FDD8445_F085

N-Channel PowerTrench[®] MOSFET

40V, 50A, 8.7mΩ

Features

- Typ $R_{DS(on)} = 6.7m\Omega$ at $V_{GS} = 10V$, $I_D = 50A$
- Typ $Q_{g(10)} = 45nC$ at $V_{GS} = 10V$, $I_D = 50A$
- Low Miller Charge
- Low Q_{rr} Body Diode
- UIS Capability (Single Pulse/ Repetitive Pulse)
- RoHS Compliant
- Qualified to AEC Q101



For current package drawing, please refer to the Fairchild website at <http://www.fairchildsemi.com/package-drawings/TO252A03.pdf>.

Applications

- Automotive Engine Control
- Powertrain Management
- Solenoid and Motor Drivers
- Electronic Transmission
- Distributed Power Architecture and VRMs
- Primary Switch for 12V Systems

MOSFET Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain to Source Voltage	40	V
V_{GS}	Gate to Source Voltage	± 20	V
I_D	Drain Current Continuous ($V_{GS} = 10V$)	50	A
	Pulsed	Figure 4	
E_{AS}	Single Pulse Avalanche Energy (Note 1)	144	mJ
P_D	Power Dissipation	79	W
	Derate above $25^\circ C$	0.53	W/ $^\circ C$
T_J, T_{STG}	Operating and Storage Temperature	-55 to +175	$^\circ C$
$R_{\theta JC}$	Thermal Resistance Junction to Case	1.9	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient, $1in^2$ copper pad area	52	$^\circ C/W$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD8445	FDD8445_F085	TO-252AA	13"	12mm	2500 units

Notes:

- 1: Starting $T_J = 25^\circ C$, $L = 0.18mH$, $I_{AS} = 40A$
- 2: A suffix as "...F085P" has been temporarily introduced in order to manage a double source strategy as Fairchild has officially announced in Aug 2014.

FDD8445_F085 N-Channel PowerTrench[®] MOSFET

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

B_{VDSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	40	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 32\text{V},$ $V_{GS} = 0\text{V}$	-	-	1	μA
		$T_A = 150^\circ\text{C}$	-	-	250	
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	2	2.8	4	V
$r_{DS(on)}$	Drain to Source On Resistance	$I_D = 50\text{A}, V_{GS} = 10\text{V}$	-	6.7	8.7	m Ω
		$I_D = 50\text{A}, V_{GS} = 10\text{V}$ $T_J = 175^\circ\text{C}$	-	12.5	16.3	

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V},$ $f = 1\text{MHz}$	-	3040	4050	pF	
C_{oss}	Output Capacitance		-	295	390	pF	
C_{rss}	Reverse Transfer Capacitance		-	178	270	pF	
R_G	Gate Resistance	$f = 1\text{MHz}$	-	1.7	-	Ω	
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0$ to 10V	$V_{DD} = 20\text{V}$ $I_D = 50\text{A}$	-	45	59	nC
$Q_{g(TH)}$	Threshold Gate Charge	$V_{GS} = 0$ to 2V		-	5.8	7.6	nC
Q_{gs}	Gate to Source Gate Charge			-	12.5	-	nC
Q_{gd}	Gate to Drain "Miller" Charge			-	10.5	-	nC

Switching Characteristics

t_{on}	Turn-On Time	$V_{DD} = 20\text{V}, I_D = 50\text{A}$ $V_{GS} = 10\text{V}, R_{GS} = 2\Omega$	-	-	138	ns
$t_{d(on)}$	Turn-On Delay Time		-	10	-	ns
t_r	Rise Time		-	82	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	26	-	ns
t_f	Fall Time		-	9.6	-	ns
t_{off}	Turn-Off Time		-	-	53	ns

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 50\text{A}$	-	-	1.25	V
		$I_{SD} = 25\text{A}$	-	-	1.0	
t_{rr}	Reverse Recovery Time	$I_{SD} = 50\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	39	ns
Q_{rr}	Reverse Recovery Charge		-	-	38	nC

Typical Characteristics

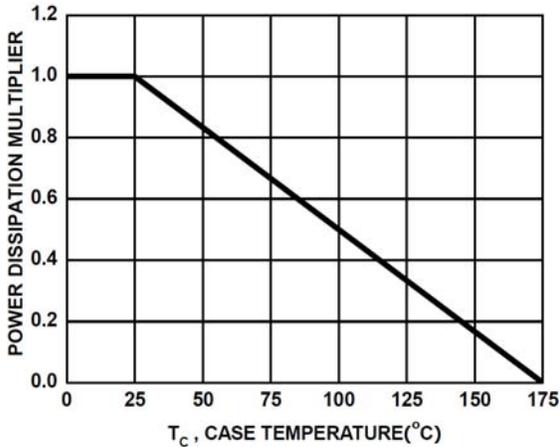


Figure 1. Normalized Power Dissipation vs Case Temperature

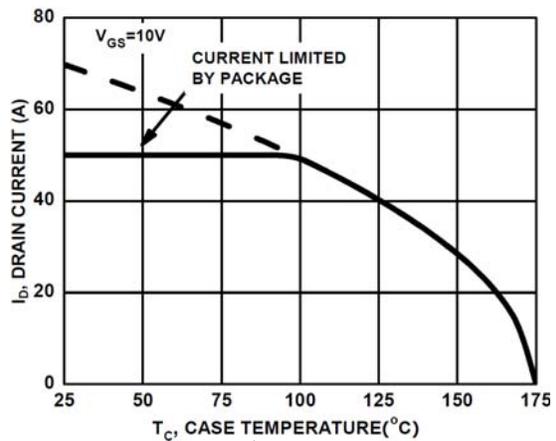


Figure 2. Maximum Continuous Drain Current vs Case Temperature

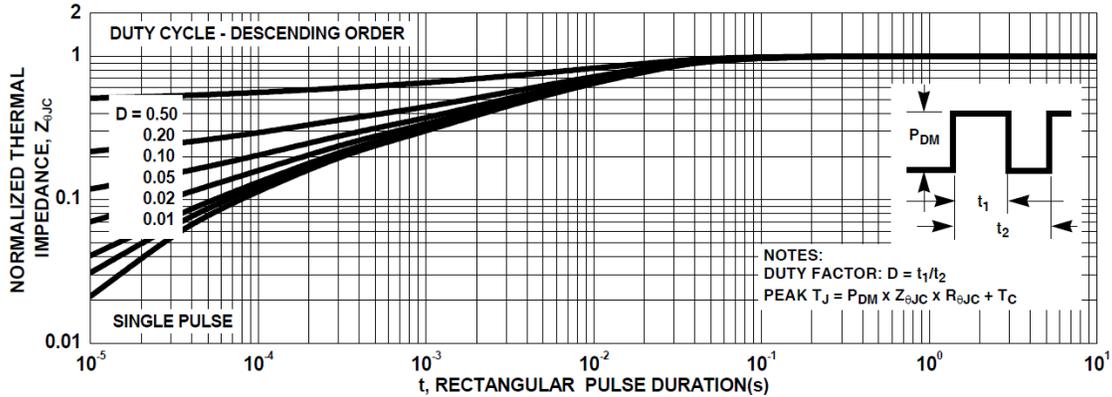


Figure 3. Normalized Maximum Transient Thermal Impedance

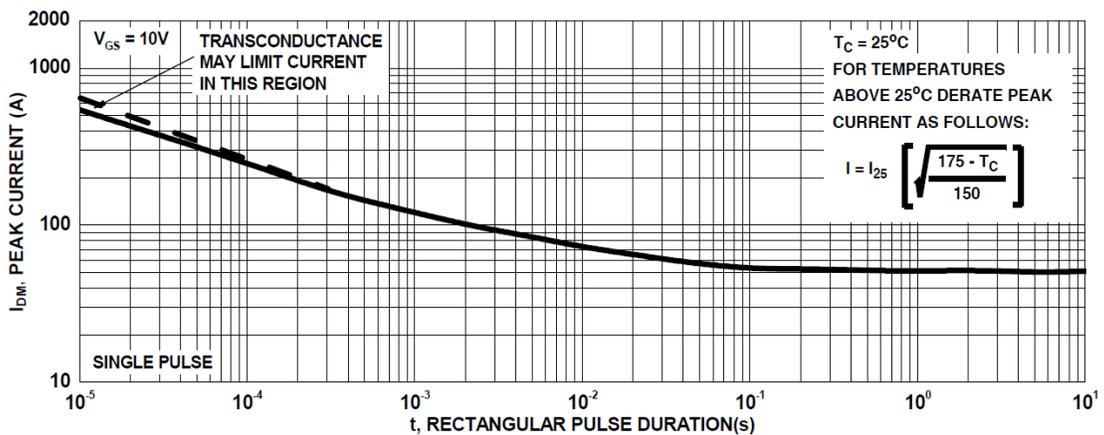


Figure 4. Peak Current Capability

Typical Characteristics

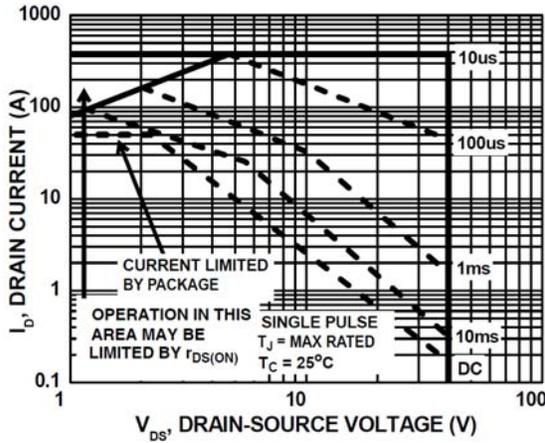
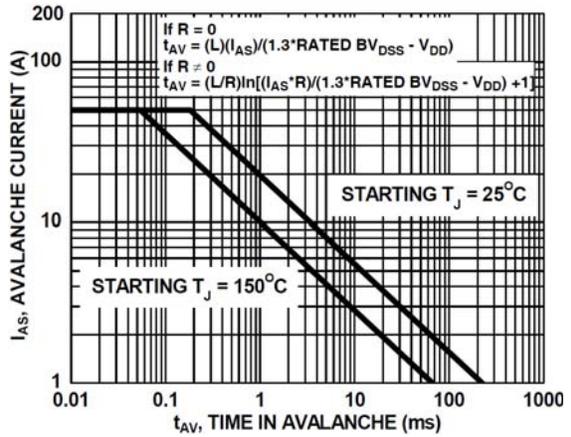


Figure 5. Forward Bias Safe Operating Area



NOTE: Refer to Fairchild Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

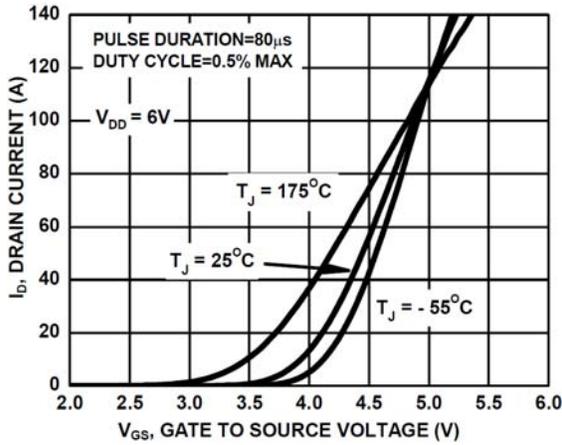


Figure 7. Transfer Characteristics

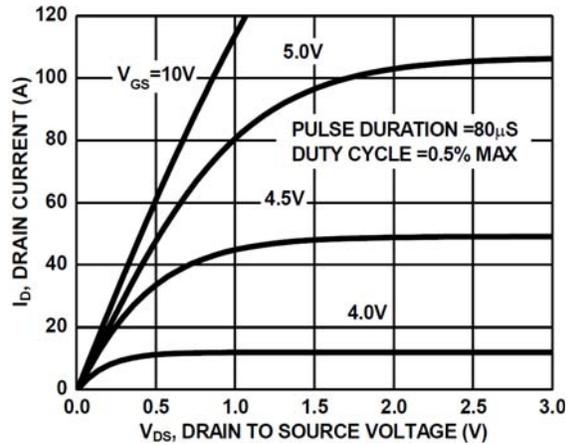


Figure 8. Saturation Characteristics

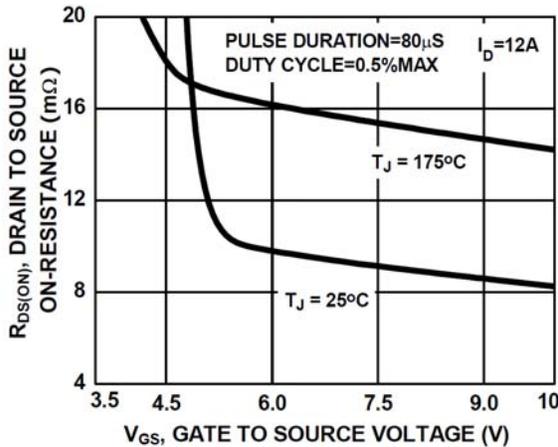


Figure 9. Drain to Source On-Resistance Variation vs Gate to Source Voltage

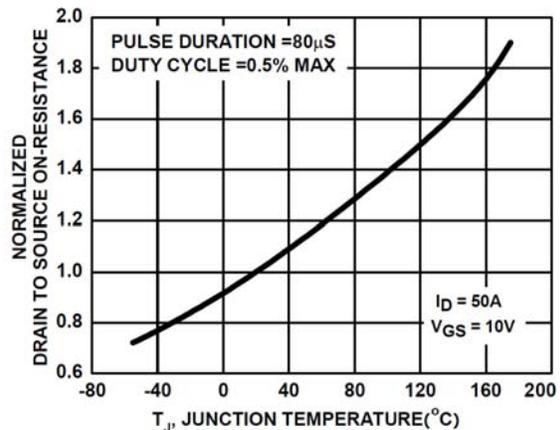


Figure 10. Normalized Drain to Source On-Resistance vs Junction Temperature

Typical Characteristics

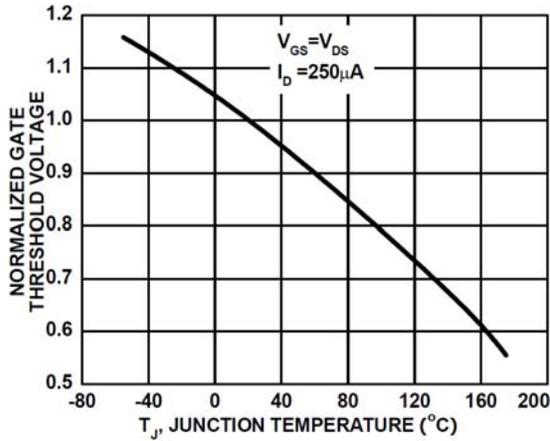


Figure 11. Normalized Gate Threshold Voltage vs Junction Temperature

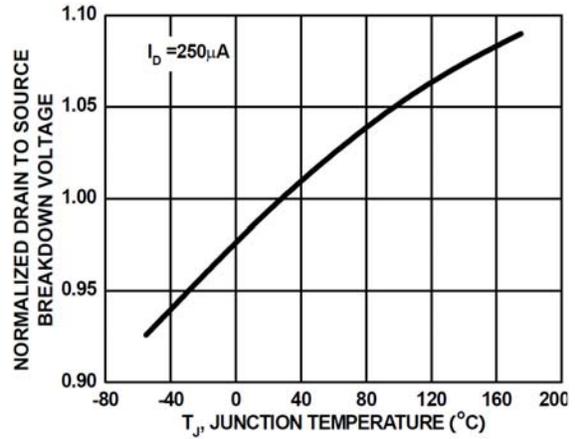


Figure 12. Normalized Drain to Source Breakdown Voltage vs Junction Temperature

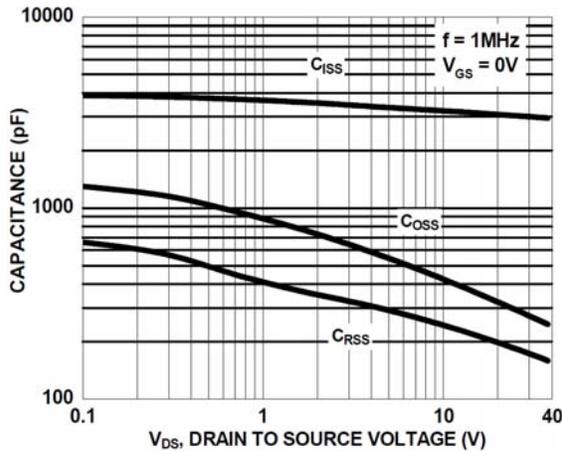


Figure 13. Capacitance vs Drain to Source Voltage

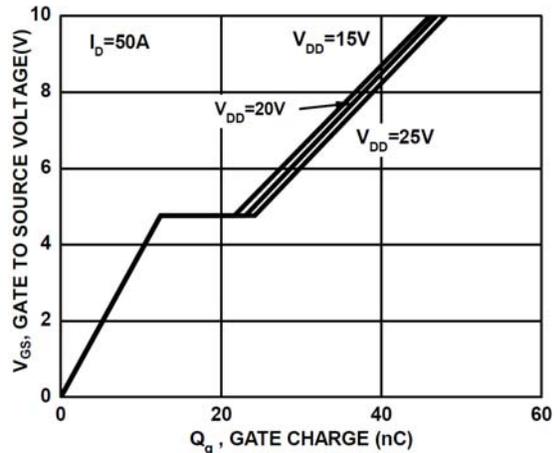
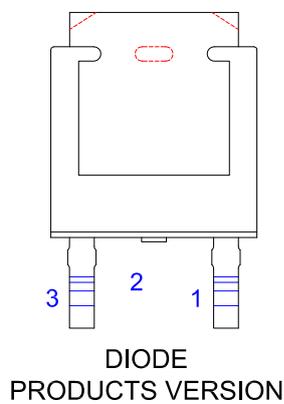
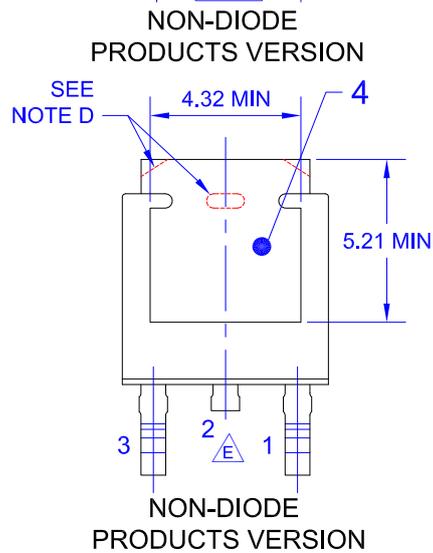
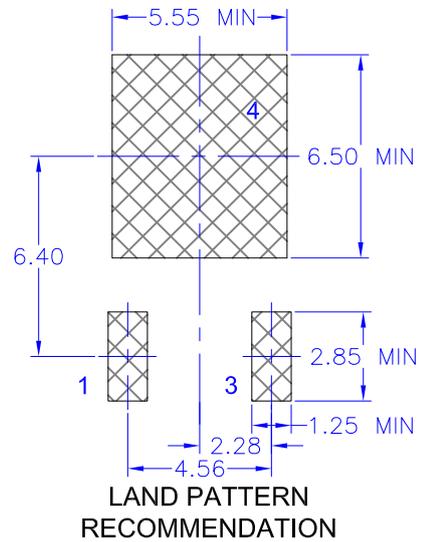
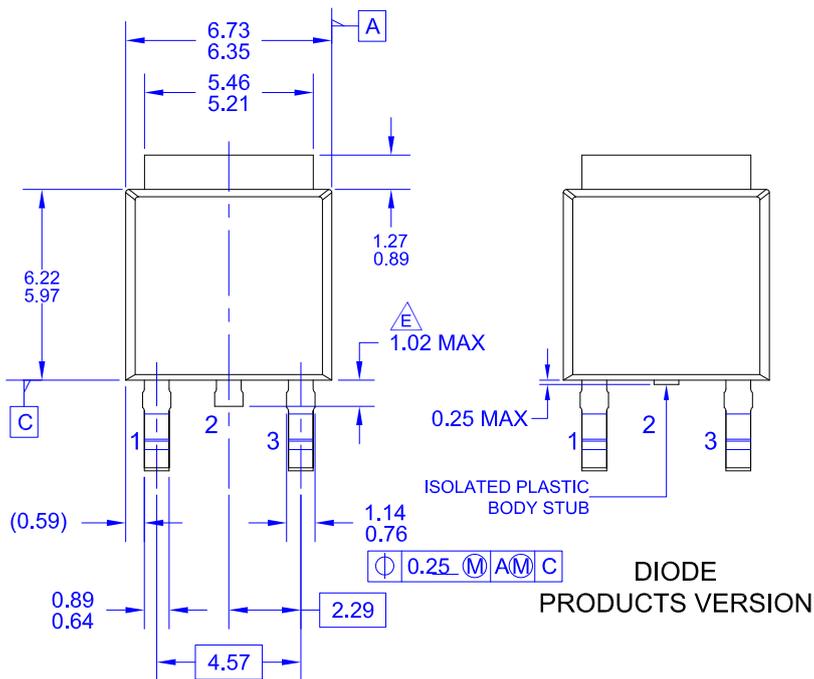


Figure 14. Gate Charge vs Gate to Source Voltage



NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.

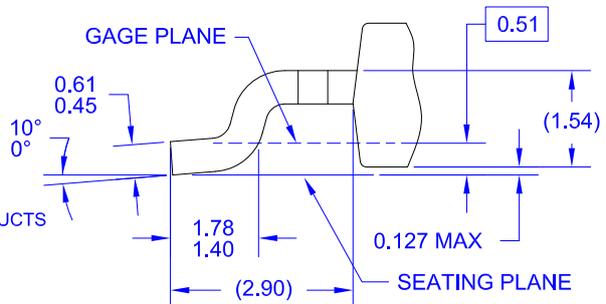
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.

E) TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS

F) DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH AND TIE BAR EXTRUSIONS.

G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.

H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11



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