International I♎R Rectifier

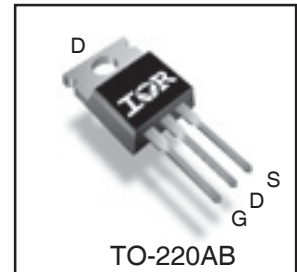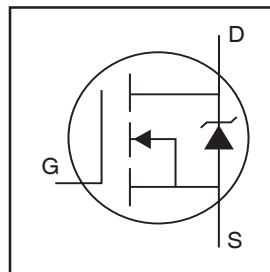**DIGITAL AUDIO MOSFET**

IRFB4019PbF

Features

- Key Parameters Optimized for Class-D Audio Amplifier Applications
- Low R_{DSON} for Improved Efficiency
- Low Q_G and Q_{SW} for Better THD and Improved Efficiency
- Low Q_{RR} for Better THD and Lower EMI
- 175°C Operating Junction Temperature for Ruggedness
- Can Deliver up to 200W per Channel into 8Ω Load in Half-Bridge Configuration Amplifier

Key Parameters		
V_{DS}	150	V
$R_{DS(ON)}$ typ. @ 10V	80	mΩ
Q_g typ.	13	nC
Q_{sw} typ.	5.1	nC
$R_{G(int)}$ typ.	2.4	Ω
T_J max	175	°C

TO-220AB

G	D	S
Gate	Drain	Source

Description

This Digital Audio MOSFET is specifically designed for Class-D audio amplifier applications. This MOSFET utilizes the latest processing techniques to achieve low on-resistance per silicon area. Furthermore, Gate charge, body-diode reverse recovery and internal Gate resistance are optimized to improve key Class-D audio amplifier performance factors such as efficiency, THD and EMI. Additional features of this MOSFET are 175°C operating junction temperature and repetitive avalanche capability. These features combine to make this MOSFET a highly efficient, robust and reliable device for ClassD audio amplifier applications.

Absolute Maximum Ratings

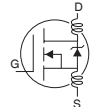|	Parameter	Max.	Units
V_{DS}	Drain-to-Source Voltage	150	V
V_{GS}	Gate-to-Source Voltage	±20	
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	17	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	12	
I_{DM}	Pulsed Drain Current ①	51	
P_D @T_C = 25°C	Power Dissipation ④	80	W
P_D @T_C = 100°C	Power Dissipation ④	40	
	Linear Derating Factor	0.5	W/°C
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw	10lb·in (1.1N·m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{θJC}$	Junction-to-Case ④	——	1.88	°C/W
$R_{θCS}$	Case-to-Sink, Flat, Greased Surface	0.50	——	
$R_{θJA}$	Junction-to-Ambient ④	——	62	

Notes ① through ⑤ are on page 2

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Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	150	——	——	V	V_{GS} = 0V, I_D = 250µA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.19	——	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	80	95	mΩ	V_{GS} = 10V, I_D = 10A ③
$V_{GS(th)}$	Gate Threshold Voltage	3.0	——	4.9	V	V_{DS} = V_{GS}, I_D = 50µA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	——	-13	——	mV/°C	
I_{DSS}	Drain-to-Source Leakage Current	——	——	20	µA	V_{DS} = 150V, V_{GS} = 0V
		——	——	250		V_{DS} = 150V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -20V
g_{fs}	Forward Transconductance	14	——	——	S	V_{DS} = 10V, I_D = 10A
Q_g	Total Gate Charge	——	13	20		
Q_{gs1}	Pre-Vth Gate-to-Source Charge	——	3.3	——		V_{DS} = 75V
Q_{gs2}	Post-Vth Gate-to-Source Charge	——	0.95	——	nC	V_{GS} = 10V
Q_{gd}	Gate-to-Drain Charge	——	4.1	——		I_D = 10A
Q_{godr}	Gate Charge Overdrive	——	4.7	——		See Fig. 6 and 19
Q_{sw}	Switch Charge (Q_{gs2} + Q_{gd})	——	5.1	——		
$R_{G(int)}$	Internal Gate Resistance	——	2.4	——	Ω	
$t_{d(on)}$	Turn-On Delay Time	——	7.0	——		V_{DD} = 75V, V_{GS} = 10V ③
t_r	Rise Time	——	13	——		I_D = 10A
$t_{d(off)}$	Turn-Off Delay Time	——	12	——	ns	R_G = 2.4Ω
t_f	Fall Time	——	7.8	——		
C_{iss}	Input Capacitance	——	800	——		V_{GS} = 0V
C_{oss}	Output Capacitance	——	74	——	pF	V_{DS} = 50V
C_{rss}	Reverse Transfer Capacitance	——	19	——		f = 1.0MHz, See Fig.5
C_{oss}	Effective Output Capacitance	——	99	——		V_{GS} = 0V, V_{DS} = 0V to 120V
L_D	Internal Drain Inductance	——	4.5	——		Between lead,
					nH	6mm (0.25in.)
L_S	Internal Source Inductance	——	7.5	——		from package
						and center of die contact

Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	——	73	mJ
I_{AR}	Avalanche Current ⑤	See Fig. 14, 15, 17a, 17b		A
E_{AR}	Repetitive Avalanche Energy ⑤			mJ

Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S @ T_C = 25°C	Continuous Source Current (Body Diode)	——	——	17	A	MOSFET symbol showing the
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	51		integral reverse
V_{SD}	Diode Forward Voltage	——	——	1.3	V	p-n junction diode. T_J = 25°C, I_S = 10A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	——	64	96	ns	T_J = 25°C, I_F = 10A
Q_{rr}	Reverse Recovery Charge	——	160	240	nC	di/dt = 100A/µs ③
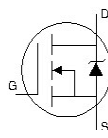
Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting T_J = 25°C, L = 1.46mH, R_G = 25Ω, I_{AS} = 10A.

③ Pulse width ≤ 400µs; duty cycle ≤ 2%.

④ R_θ is measured at T_J of approximately 90°C.

⑤ Limited by Tjmax. See Figs. 14, 15, 17a, 17b for repetitive avalanche information

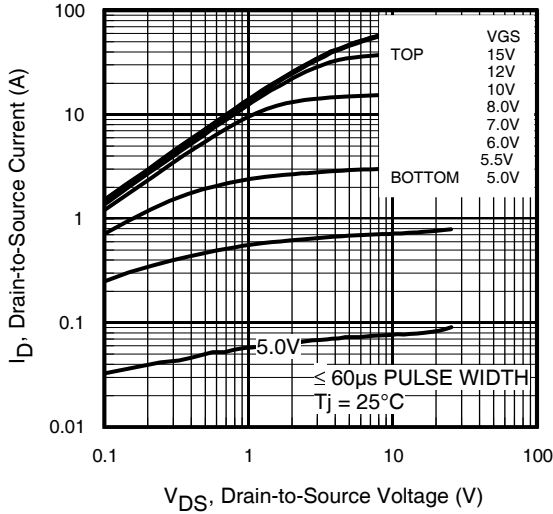International **IoR** Rectifier

IRFB4019PbF

Fig 1. Typical Output Characteristics
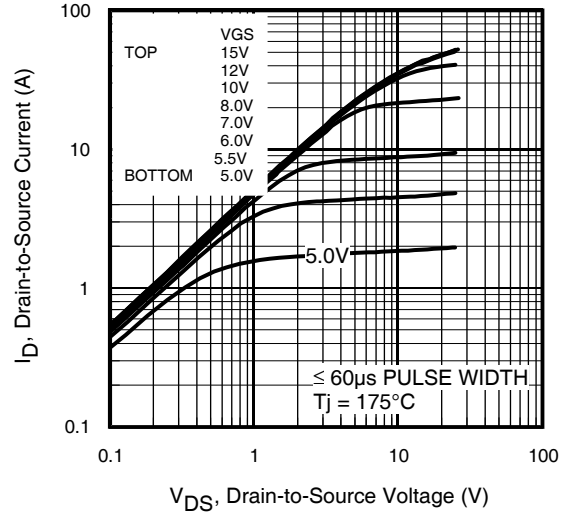

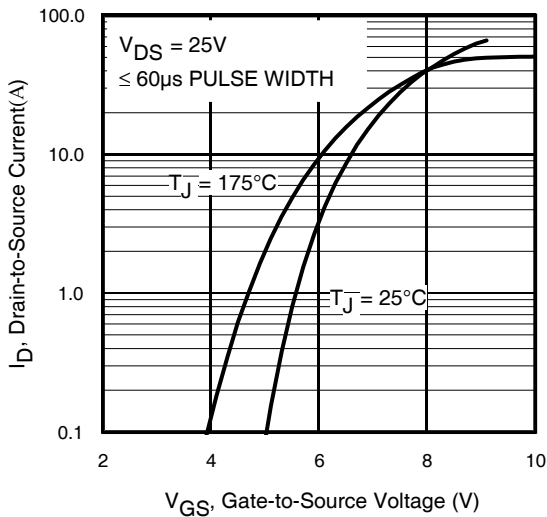**Fig 2.** Typical Output Characteristics
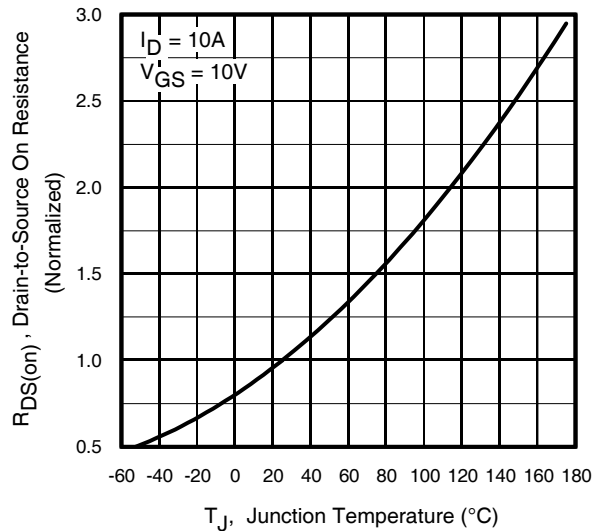

Fig 3. Typical Transfer Characteristics

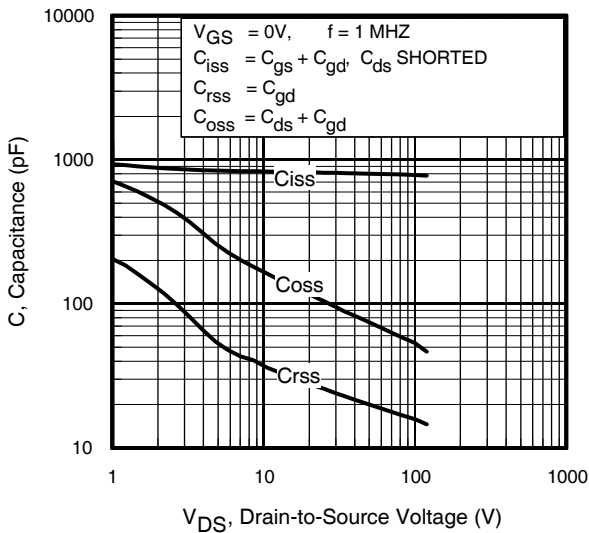**Fig 4.** Normalized On-Resistance vs. Temperature

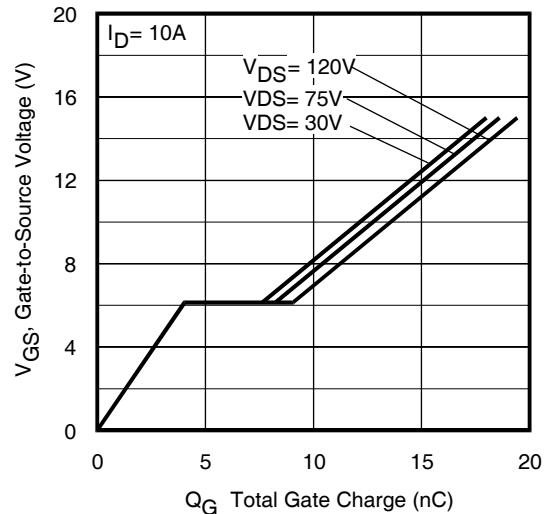**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage

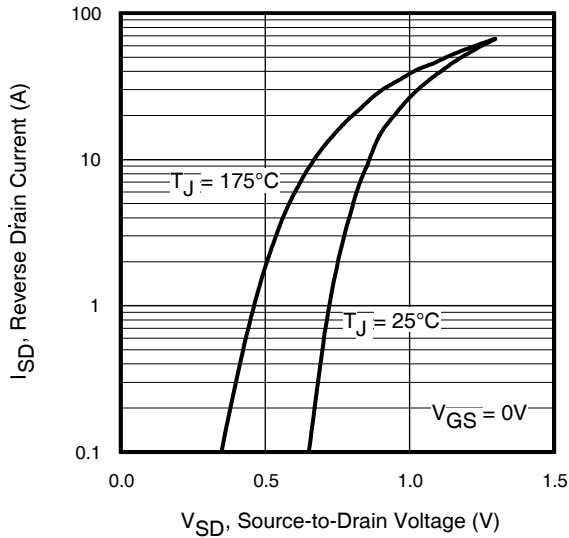**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage

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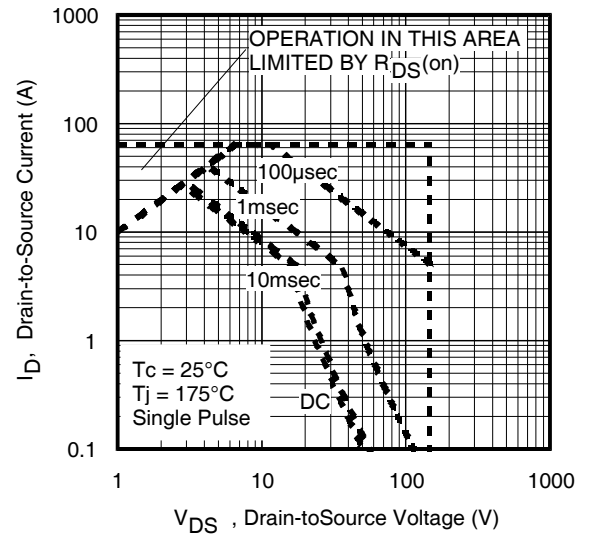
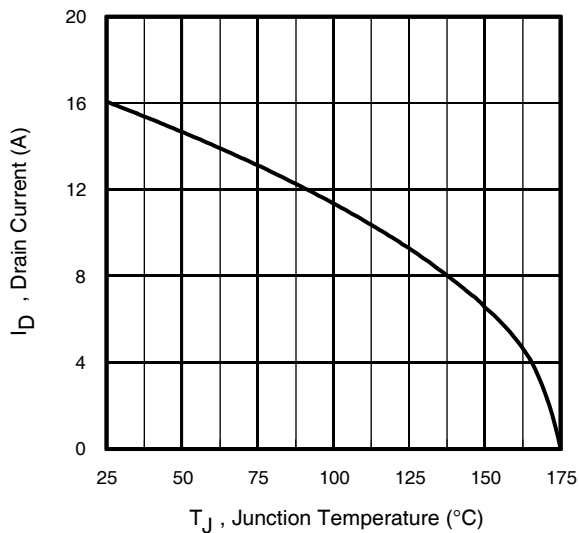**Fig 7.** Typical Source-Drain Diode Forward Voltage

Fig 8. Maximum Safe Operating Area
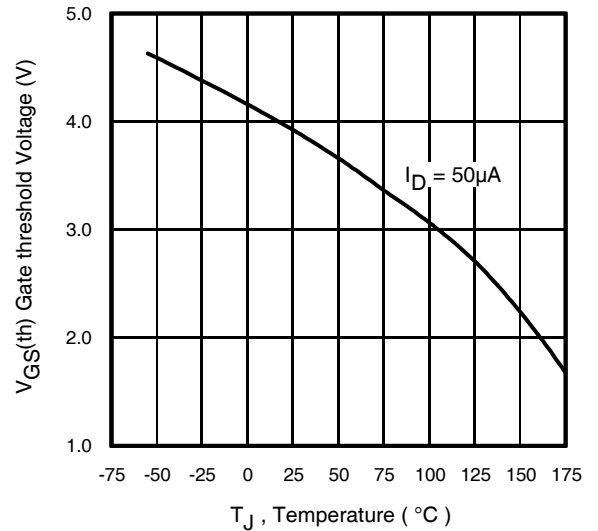

Fig 9. Maximum Drain Current vs. Case Temperature
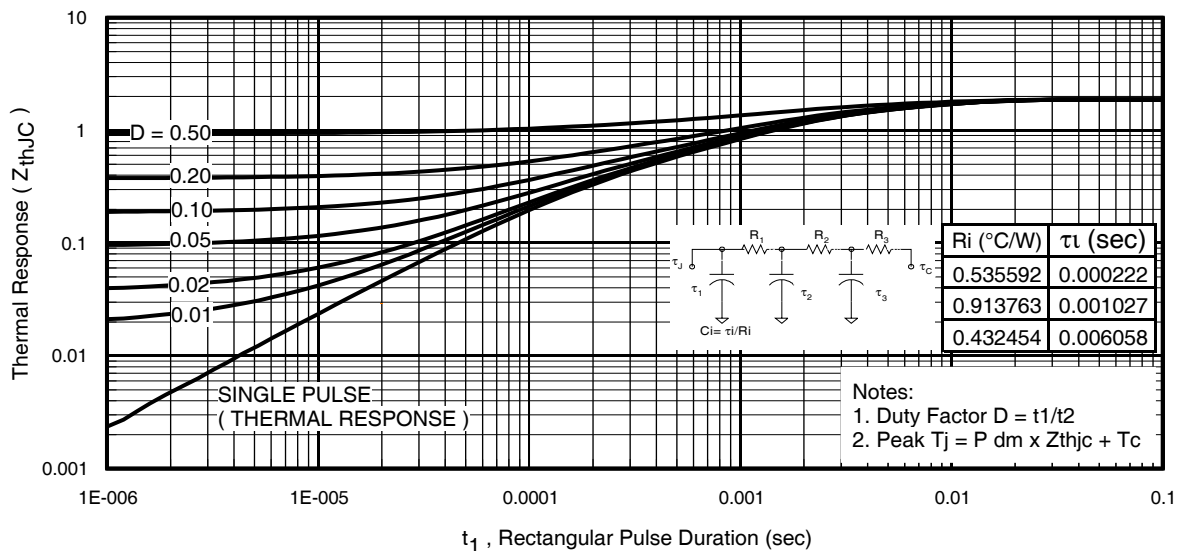

Fig 10. Threshold Voltage vs. Temperature

Ri (°C/W)	τι (sec)
0.535592	0.000222
0.913763	0.001027
0.432454	0.006058

Notes:
1. Duty Factor D = t1/t2
2. Peak Tj = P dm x Zthjc + Tc

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

4
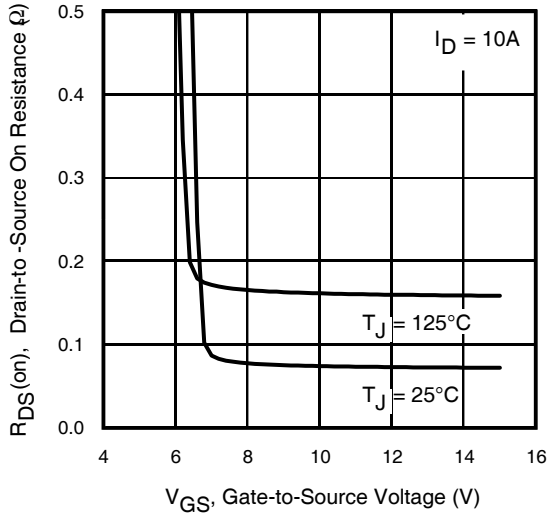
www.irf.com

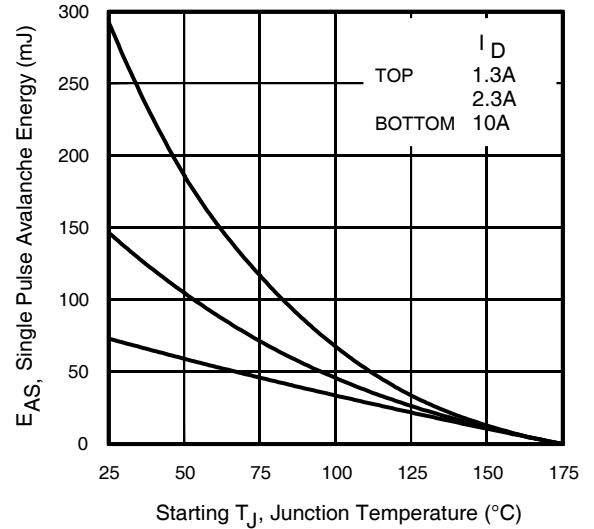**Fig 12.** On-Resistance Vs. Gate Voltage

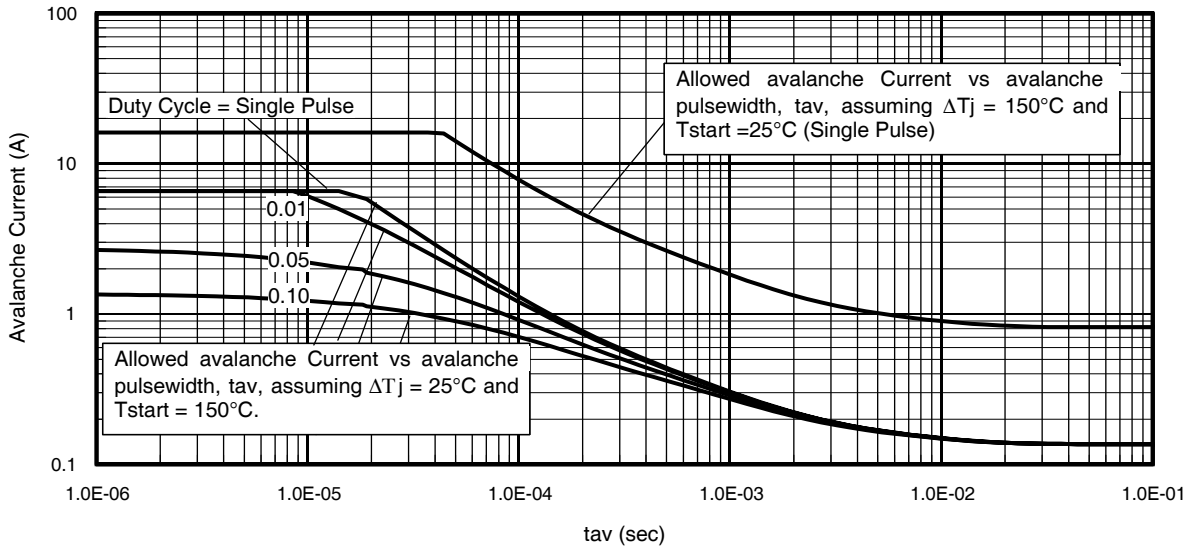**Fig 13.** Maximum Avalanche Energy Vs. Drain Current

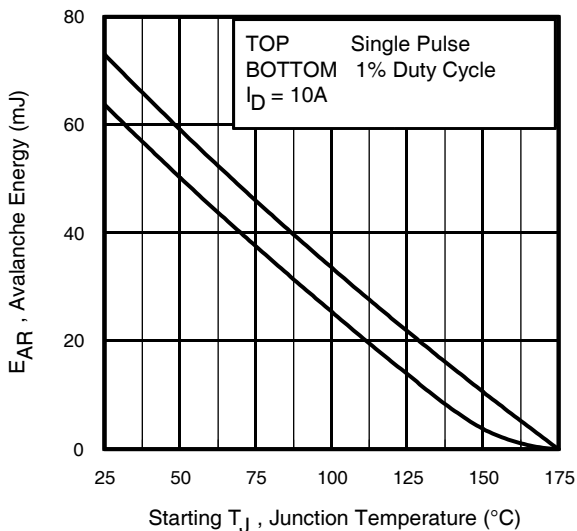**Fig 14.** Typical Avalanche Current Vs.Pulsewidth

Fig 15. Maximum Avalanche Energy Vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax}. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as neither Tjmax nor Iav (max) is exceeded
3. Equation below based on circuit and waveforms shown in Figures 17a, 17b.
4. $P_{D (ave)}$ = Average power dissipation per single avalanche pulse.
5. B_V = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
   t_{av} = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see figure 11)

$$P_{D (ave)} = 1/2 \ (\ 1.3 \cdot BV \cdot I_{av}) = \Delta T / \ Z_{thJC}$$
$$I_{av} = 2\Delta T / \ [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS (AR)} = P_{D (ave)} \cdot t_{av}$$

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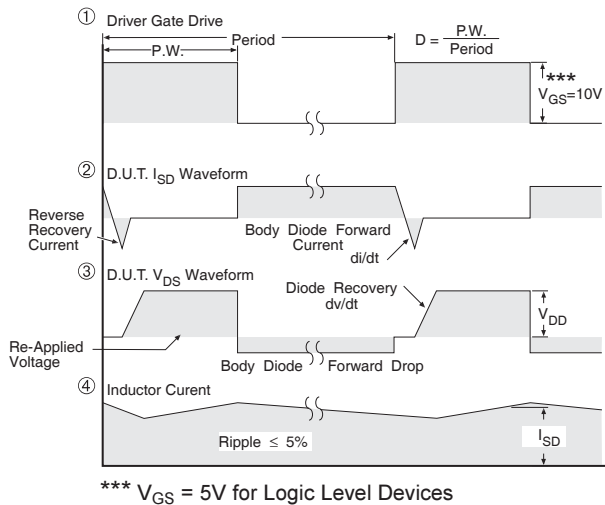
Circuit Layout Considerations
- Low Stray Inductance
- Ground Plane
- Low Leakage Inductance Current Transformer

- dv/dt controlled by R_G
- Driver same type as D.U.T.
- I_{SD} controlled by Duty Factor "D"
- D.U.T. - Device Under Test

* Use P-Channel Driver for P-Channel Measurements
** Reverse Polarity for P-Channel

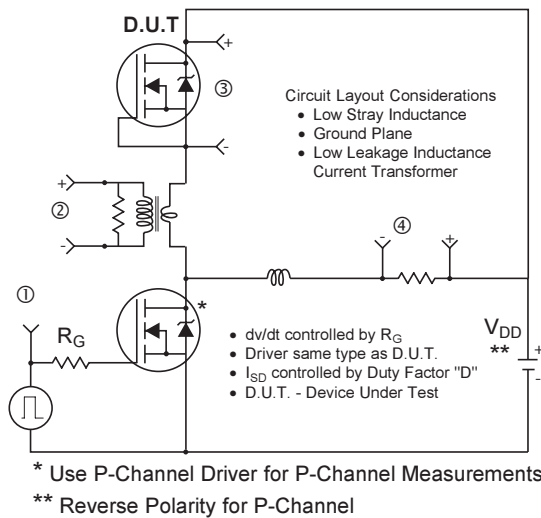*** V_{GS} = 5V for Logic Level Devices

Fig 16. Diode Reverse Recovery Test Circuit for HEXFET® Power MOSFETs
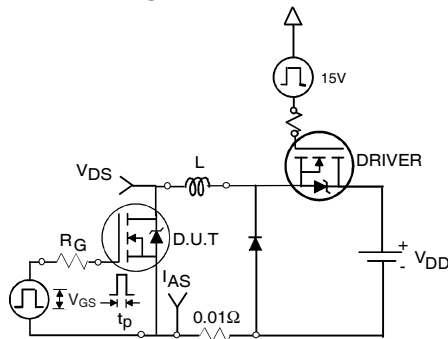

Fig 17a. Unclamped Inductive Test Circuit
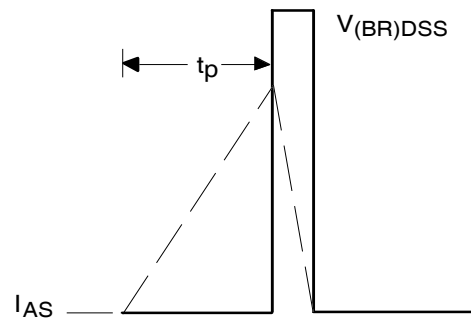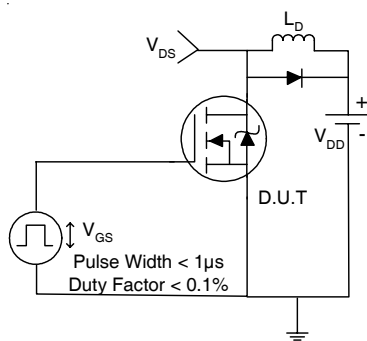
Fig 17b. Unclamped Inductive Waveforms
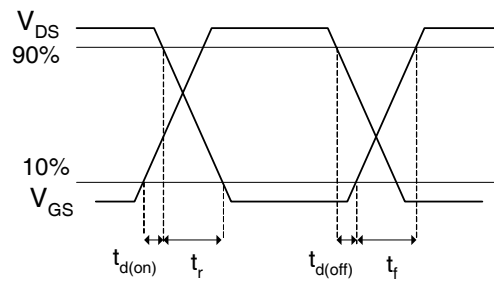

Fig 18a. Switching Time Test Circuit
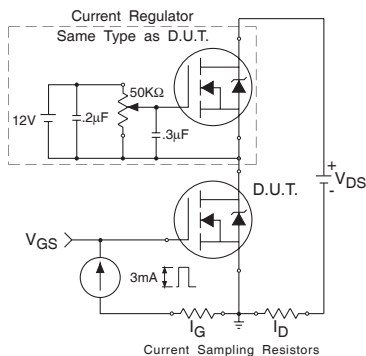
Fig 18b. Switching Time Waveforms

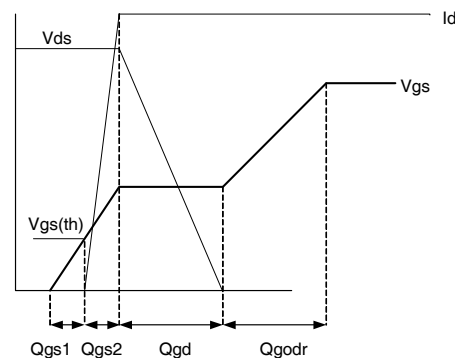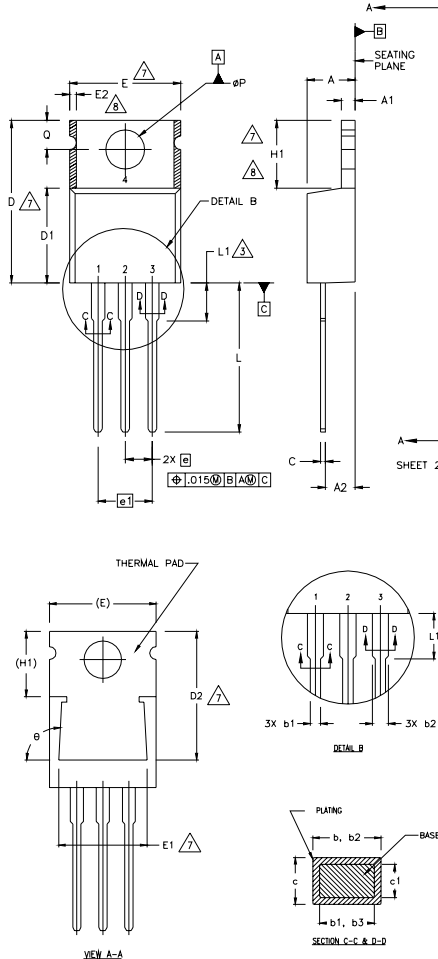**Fig 19a.** Gate Charge Test Circuit

Fig 19b Gate Charge Waveform

TO-220AB Package Outline (Dimensions are shown in millimeters (inches))

NOTES:
1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M– 1994.
2 DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
3 LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
4 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5 DIMENSION b1 & c1 APPLY TO BASE METAL ONLY.
6 CONTROLLING DIMENSION : INCHES.
7 THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E,H1,D2 & E1
8 DIMENSION E2 X H1 DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.

LEAD ASSIGNMENTS

HEXFET
1.– GATE
2.– DRAIN
3.– SOURCE

IGBTs, CoPACK
1.– GATE
2.– COLLECTOR
3.– EMITTER

DIODES
1.– ANODE/OPEN
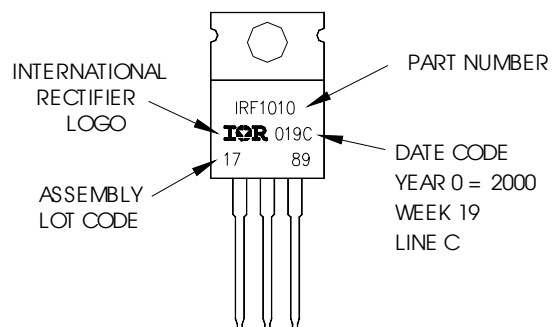2.– CATHODE
3.– ANODE

SYMBOL	DIMENSIONS				
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	NOTES
A	3.56	4.82	.140	.190	
A1	0.51	1.40	.020	.055	
A2	2.04	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.96	.015	.038	5
b2	1.15	1.77	.045	.070	
b3	1.15	1.73	.045	.068	
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	12.19	12.88	.480	.507	7
E	9.66	10.66	.380	.420	4,7
E1	8.38	8.89	.330	.350	7
e	2.54 BSC		.100 BSC		
e1	5.08		.200 BSC		
H1	5.85	6.55	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	–	6.35	–	.250	3
øP	3.54	4.08	.139	.161	
Q	2.54	3.42	.100	.135	
ø	90°–93°		90°–93°		

TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010
LOT CODE 1789
ASSEMBLED ON WW 19, 2000
IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead - Free"

INTERNATIONAL RECTIFIER LOGO

PART NUMBER

DATE CODE
YEAR 0 = 2000
WEEK 19
LINE C

ASSEMBLY LOT CODE

TO-220AB packages are not recommended for Surface Mount Application.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualification Standards can be found on IR's Web site.

International IOR Rectifier

Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/