

# **FDD6688S**

# **30V N-Channel PowerTrench® SyncFET™**

### **General Description**

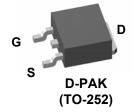
The FDD6688S is designed to replace a single TO-252 MOSFET and Schottky diode in synchronous DC:DC power supplies. This 30V MOSFET is designed to maximize power conversion efficiency, providing a low  $R_{\text{DS}(\text{ON})}$  and low gate charge. The FDD6688S includes an integrated Schottky diode using Fairchild's monolithic SyncFET technology.

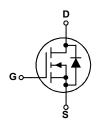
### Applications

- DC/DC converter
- Motor Drives

### **Features**

- 88 A, 30 V.  $R_{DS(ON)} = 5.1 \text{ m}\Omega \text{ @ V}_{GS} = 10 \text{ V}$  $R_{DS(ON)} = 6.3 \text{ m}\Omega \text{ @ V}_{GS} = 4.5 \text{ V}$
- Low gate charge (31 nC typical)
- · Fast switching
- High performance trench technology for extremely low R<sub>DS(ON)</sub>





Absolute Maximum Ratings TA=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V <sub>DSS</sub>	Drain-Source Voltage		30	V
V <sub>GSS</sub>	Gate-Source Voltage		± 20	
I <sub>D</sub>	Drain Current - Continuous	(Note 3)	88	A
	- Pulsed	(Note 1a)	100	
P <sub>D</sub>	Power Dissipation for Single Operation	(Note 1)	69	W
		(Note 1a)	3.1	
		(Note 1b)	1.3	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperat	ure Range	-55 to +150	°C

### **Thermal Characteristics**

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	1.8	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	40	
		(Note 1b)	96	

**Package Marking and Ordering Information** 

Device Marking	Device	Package	Reel Size	Tape width	Quantity	
FDD6688S	FDD6688S	D-PAK (TO-252)	13"	12mm	2500 units	

Symbol	Parameter	Test Conditions		Тур	Max	Units
Drain-So	urce Avalanche Ratings (No	te 2)	1	l	Į.	
W <sub>DSS</sub>	Drain-Source Avalanche Energy	Single Pulse, $V_{DD} = 15 \text{ V}$ , $I_D = 21 \text{ A}$		501		mJ
I <sub>AR</sub>	Drain-Source Avalanche Current	-			21	Α
Off Char	acteristics		•			
BV <sub>DSS</sub>	Drain–Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, \qquad I_D = 1\text{mA}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 10mA, Referenced to 25°C		24		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 24 V, V <sub>GS</sub> = 0 V			500	μΑ
I <sub>GSS</sub>	Gate-Body Leakage	$V_{GS} = \pm 20 \text{ V},  V_{DS} = 0 \text{ V}$			± 100	nA
On Char	acteristics (Note 2)					
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 1mA$	1	1.4	3	V
$\Delta V_{GS(th)} \over \Delta T_{,J}$	Gate Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 10mA, Referenced to 25°C		-4		mV/°C
R <sub>DS(on)</sub>	Static Drain–Source On–Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 18.5 A V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 16.5 A V <sub>GS</sub> = 10 V, I <sub>D</sub> = 18.5 A, T <sub>J</sub> =125°C		4.0 4.7 6.0	5.1 6.3 7.5	mΩ
<b>g</b> <sub>FS</sub>	Forward Transconductance	$V_{DS} = 5 \text{ V}, \qquad I_{D} = 18.5 \text{ A}$		72		S
Dvnamic	Characteristics					
C <sub>iss</sub>	Input Capacitance			3290		pF
Coss	Output Capacitance	$V_{DS} = 15 \text{ V}, \qquad V_{GS} = 0 \text{ V},$		900		pF
C <sub>rss</sub>	Reverse Transfer Capacitance	f = 1.0 MHz		300		pF
R <sub>G</sub>	Gate Resistance	V <sub>GS</sub> = 15 mV, f = 1.0 MHz		1.6		Ω
Switchin	g Characteristics (Note 2)					
t <sub>d(on)</sub>	Turn–On Delay Time			13	23	ns
t <sub>r</sub>	Turn–On Rise Time	$V_{DD} = 15 \text{ V}, \qquad I_D = 1 \text{ A},$		13	23	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, \qquad R_{GEN} = 6 \Omega$		31	50	ns
t <sub>f</sub>	Turn-Off Fall Time			64	103	ns
Q <sub>g(TOT)</sub>	Total Gate Charge at Vgs=10V			58	81	nC
Q <sub>g</sub>	Total Gate Charge at Vgs=5V	V -15V   -105A		31	44	nC
Q <sub>gs</sub>	Gate-Source Charge	$V_{DD} = 15 \text{ V},  I_D = 18.5 \text{ A}$		8		nC
$Q_{gd}$	Gate-Drain Charge			10		nC

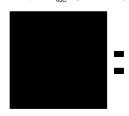
# **Electrical Characteristics** (continued)

T<sub>A</sub> = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Drain-Sc	Drain-Source Diode Characteristics and Maximum Ratings					
V <sub>SD</sub>	Drain–Source Diode Forward Voltage	$V_{GS} = 0 \text{ V},  I_S = 4.4 \text{ A}  \text{(Note 2)}$		400	700	mV
t <sub>rr</sub>	Diode Reverse Recovery Time			28		ns
Q <sub>rr</sub>	Diode Reverse Recovery Charge	$I_F = 18.5 \text{ A},  d_{iF}/d_t = 300 \text{ A/}\mu\text{s}$		30		nC
Im	Diode Reverse Recovery Current			2.1		Α

#### Notes:8

R<sub>0JA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of
the drain pins. R<sub>0JC</sub> is guaranteed by design while R<sub>0CA</sub> is determined by the user's board design.



a)  $R_{\theta,JA} = 40^{\circ}\text{C/W}$  when mounted on a  $1\text{in}^2$  pad of 2 oz copper



b)  $R_{\theta JA} = 96^{\circ}C/W$  when mounted on a minimum pad.

Scale 1:1 on letter size paper

2. Pulse Test: Pulse Width < 300 $\mu$ s, Duty Cycle < 2.0%

3. Maximum current is calculated as:  $\sqrt{\frac{P_D}{R_{DS(ON)}}}$ 

where  $P_D$  is maximum power dissipation at  $T_C$  = 25°C and  $R_{DS(on)}$  is at  $T_{J(max)}$  and  $V_{GS}$  = 10V. Package current limitation is 21A

# **Typical Characteristics**

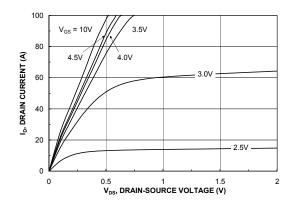


Figure 1. On-Region Characteristics.

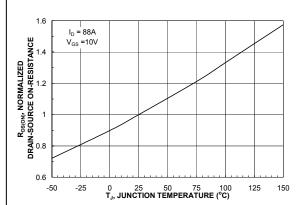


Figure 3. On-Resistance Variation with Temperature.

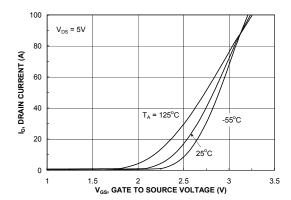


Figure 5. Transfer Characteristics

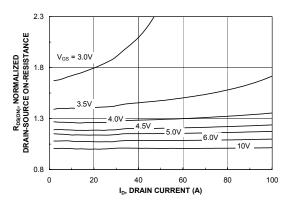


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

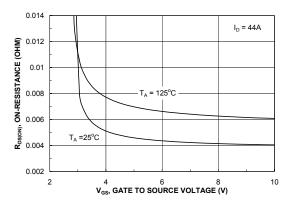


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

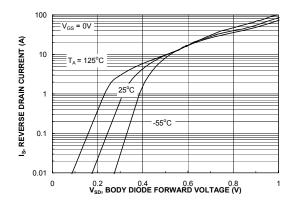
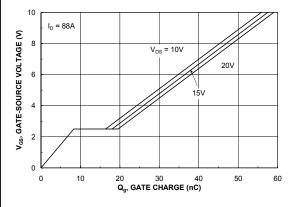


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

# **Typical Characteristics**



5000 | f = 1MHz | V<sub>GS</sub> = 0 V |

4000 | C<sub>Iss</sub> | C<sub>Iss</sub> |

1000 | C<sub>rss</sub> | C<sub>Iss</sub> |

1000 | C<sub>rss</sub> | C<sub>Iss</sub> | C<sub>Iss</sub> |

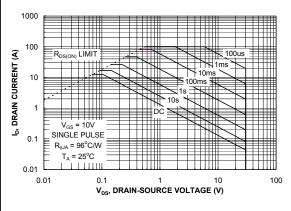
1000 | C<sub>Iss</sub> | C<sub>Iss</sub> | C<sub>Iss</sub> |

1000 | C<sub>Iss</sub> | C<sub>Iss</sub> | C<sub>Iss</sub> | C<sub>Iss</sub> | C<sub>Iss</sub> |

1000 | C<sub>Iss</sub> | C<sub>Is</sub>

Figure 7. Gate Charge Characteristics





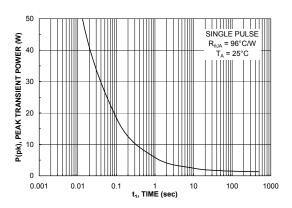


Figure 9. Maximum Safe Operating Area

Figure 10. Single Pulse Maximum Power Dissipation

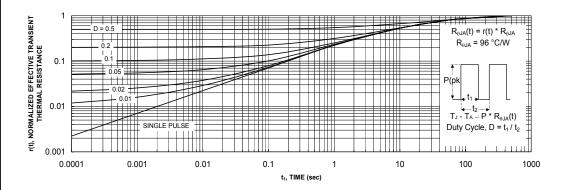


Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

### Typical Characteristics (continued)

# SyncFET Schottky Body Diode Characteristics

Fairchild's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 12 shows the reverse recovery characteristic of the FDD6688S.

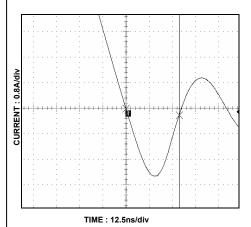


Figure 12. FDD6688S SyncFET body diode reverse recovery characteristic.

For comparison purposes, Figure 13 shows the reverse recovery characteristics of the body diode of an equivalent size MOSFET produced without SyncFET (FDD6688).

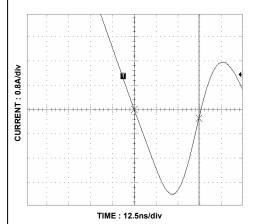


Figure 13. Non-SyncFET (FDD6688) body diode reverse recovery characteristic.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

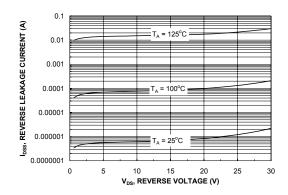
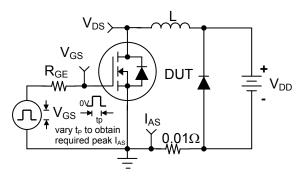


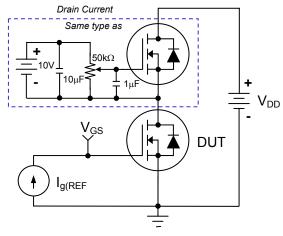
Figure 14. SyncFET body diode reverse leakage versus drain-source voltage and temperature.



BV<sub>DSS</sub> V<sub>DS</sub> V<sub>DD</sub>

Figure 15. Unclamped Inductive Load Test Circuit

Figure 16. Unclamped Inductive Waveforms



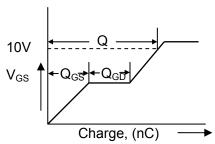
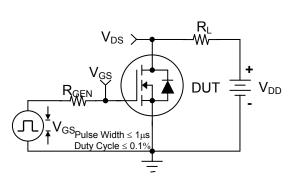


Figure 17. Gate Charge Test Circuit

Figure 18. Gate Charge Waveform



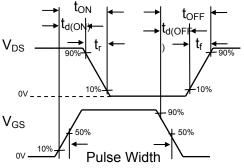


Figure 19. Switching Time Test Circuit

Figure 20. Switching Time Waveforms





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