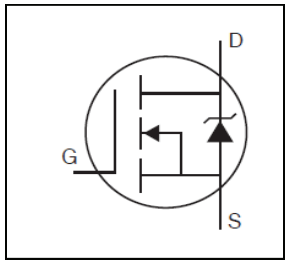
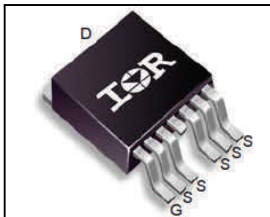
| | |
|---|---|
| $V_{DSS}$ | 40V |
| $R_{DS(on)}$ typ. | 0.50mΩ |
| max. | 0.69mΩ |
| $I_D$ (Silicon Limited) | 523A① |
| $I_D$ (Package Limited) | 360A |



D[2]PAK-7TP

| G | D | S |
|---|---|---|
| Gate | Drain | Source |

### Features
- Advanced Process Technology
- New Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified *

### Description
Specifically designed for Automotive applications, this HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and wide variety of other applications.

### Applications
- Electric Power Steering (EPS)
- Battery Switch
- Start/Stop Micro Hybrid
- Heavy Loads
- DC-DC Applications

| Base Part Number | Package Type | Standard Pack | | Complete Part Number |
|---|---|---|---|---|
| | | Form | Quantity | |
| AUIRFSA8409-7P | D[2]PAK-7TP | Tube | 50 | AUIRFSA8409-7P |
| | | Tape and Reel Left | 800 | AUIRFSA8409-7TRL |

### Absolute Maximum Ratings
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

| Symbol | Parameter | Max. | Units |
|---|---|---|---|
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10V (Silicon Limited) | 523① | A |
| $I_D$ @ $T_C$ = 100°C | Continuous Drain Current, $V_{GS}$ @ 10V (Silicon Limited) | 370① | |
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10V (Wire Bond Limited) | 360 | |
| $I_{DM}$ | Pulsed Drain Current ② | 1440* | |
| $P_D$ @$T_C$ = 25°C | Maximum Power Dissipation | 375 | W |
| | Linear Derating Factor | 2.5 | W/°C |
| $V_{GS}$ | Gate-to-Source Voltage | ± 20 | V |
| $T_J$<br>$T_{STG}$ | Operating Junction and<br>Storage Temperature Range | -55 to + 175 | °C |
| | Soldering Temperature, for 10 seconds (1.6mm from case) | 300 | |

### Avalanche Characteristics

| | | | |
|---|---|---|---|
| $E_{AS}$ (Thermally Limited) | Single Pulse Avalanche Energy ③ | 743 | mJ |
| $E_{AS}$ (Thermally Limited) | Single Pulse Avalanche Energy ⑩ | 1450 | |
| $I_{AR}$ | Avalanche Current ② | See Fig. 14, 15, 24a, 24b | A |
| $E_{AR}$ | Repetitive Avalanche Energy ② | | mJ |

HEXFET® is a registered trademark of Infineon.
*Qualification standards can be found at www.infineon.com

## Thermal Resistance

| Symbol | Parameter | Typ. | Max. | Units |
|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-Case ⑨ | —— | 0.4 | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient (PCB Mount) ⑧ | —— | 40 | |

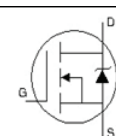
## Static Electrical Characteristics @ $T_J$ = 25°C (unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 40 | —— | —— | V | $V_{GS}$ = 0V, $I_D$ = 250μA |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | —— | 0.038 | —— | V/°C | Reference to 25°C, $I_D$ = 2.0mA② |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | —— | 0.50 | 0.69 | mΩ | $V_{GS}$ = 10V, $I_D$ = 100A ⑤ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 2.2 | 3.0 | 3.9 | V | $V_{DS}$ = $V_{GS}$, $I_D$ = 250μA |
| $I_{DSS}$ | Drain-to-Source Leakage Current | —— | —— | 1.0 | μA | $V_{DS}$ = 40V, $V_{GS}$ = 0V |
| | | —— | —— | 150 | | $V_{DS}$ = 40V, $V_{GS}$ = 0V, $T_J$ = 125°C |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | —— | —— | 100 | nA | $V_{GS}$ = 20V |
| | Gate-to-Source Reverse Leakage | —— | —— | -100 | | $V_{GS}$ = -20V |
| $R_G$ | Internal Gate Resistance | —— | 2.3 | —— | Ω | |

## Dynamic Electrical Characteristics @ $T_J$ = 25°C (unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| gfs | Forward Transconductance | 180 | —— | —— | S | $V_{DS}$ = 10V, $I_D$ = 100A |
| $Q_g$ | Total Gate Charge | —— | 305 | 460 | nC | $I_D$ = 100A |
| $Q_{gs}$ | Gate-to-Source Charge | —— | 84 | —— | | $V_{DS}$ = 20V |
| $Q_{gd}$ | Gate-to-Drain ("Miller") Charge | —— | 96 | —— | | $V_{GS}$ = 10V ⑤ |
| $Q_{sync}$ | Total Gate Charge Sync. ($Q_g$ - $Q_{gd}$) | —— | 209 | —— | | |
| $t_{d(on)}$ | Turn-On Delay Time | —— | 21 | —— | ns | $V_{DD}$ = 20V |
| $t_r$ | Rise Time | —— | 94 | —— | | $I_D$ = 100A |
| $t_{d(off)}$ | Turn-Off Delay Time | —— | 150 | —— | | $R_G$ = 2.7Ω |
| $t_f$ | Fall Time | —— | 90 | —— | | $V_{GS}$ = 10V ⑤ |
| $C_{iss}$ | Input Capacitance | —— | 13975 | —— | pF | $V_{GS}$ = 0V |
| $C_{oss}$ | Output Capacitance | —— | 2140 | —— | | $V_{DS}$ = 25V |
| $C_{rss}$ | Reverse Transfer Capacitance | —— | 1438 | —— | | $f$ = 1.0 MHz |
| $C_{oss}$ eff. (ER) | Effective Output Capacitance (Energy Related) ⑦ | —— | 2620 | —— | | $V_{GS}$ = 0V, $V_{DS}$ = 0V to 32V ⑦ |
| $C_{oss}$ eff. (TR) | Effective Output Capacitance (Time Related)⑥ | —— | 3306 | —— | | $V_{GS}$ = 0V, $V_{DS}$ = 0V to 32V ⑥ |

## Diode Characteristics

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | —— | —— | 523① | A | MOSFET symbol showing the integral reverse p-n junction diode.  |
| $I_{SM}$ | Pulsed Source Current (Body Diode) ② | —— | —— | 1440* | A | |
| $V_{SD}$ | Diode Forward Voltage | —— | 0.8 | 1.3 | V | $T_J$ = 25°C, $I_S$ = 100A, $V_{GS}$ = 0V ⑤ |
| dv/dt | Peak Diode Recovery ④ | —— | 3.1 | —— | V/ns | $T_J$ = 175°C, $I_S$ = 100A, $V_{GS}$ = 40V |
| $t_{rr}$ | Reverse Recovery Time | —— | 59 | —— | ns | $T_J$ = 25°C; $V_R$ = 34V, $I_F$ = 100A, di/dt = 100A/μs⑤ |
| | | —— | 60 | —— | | $T_J$ = 125°C |
| $Q_{rr}$ | Reverse Recovery Charge | —— | 96 | —— | nC | $T_J$ = 25°C |
| | | —— | 98 | —— | | $T_J$ = 125°C |
| $I_{RRM}$ | Reverse Recovery Current | —— | 2.7 | —— | A | $T_J$ = 25°C |

**Notes:**

① Calculated continuous current based on maximum allowable junction temperature. Bond wire current limit is 360A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements. (Refer to AN-1140)

② Repetitive rating; pulse width limited by max. junction temperature.

③ Limited by $T_{Jmax}$, starting $T_J$ = 25°C, L = 0.15mH $R_G$ = 50Ω, $I_{AS}$ = 100A, $V_{GS}$ =10V.

④ $I_{SD}$ ≤ 100A, di/dt ≤ 1070A/μs, $V_{DD}$ ≤ $V_{(BR)DSS}$, $T_J$ ≤ 175°C.

⑤ Pulse width ≤ 400μs; duty cycle ≤ 2%.

⑥ $C_{oss}$ eff. (TR) is a fixed capacitance that gives the same charging time as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$.

⑦ $C_{oss}$ eff. (ER) is a fixed capacitance that gives the same energy as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$.

⑧ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.

⑨ $R_\theta$ is measured at $T_J$ approximately 90°C.

⑩ Limited by $T_{Jmax}$, starting $T_J$ = 25°C, L = 1mH, $R_G$ = 50Ω, $I_{AS}$ = 53A, $V_{GS}$ =10V.

* Pulse drain current is limited to 1440A by source bonding technology

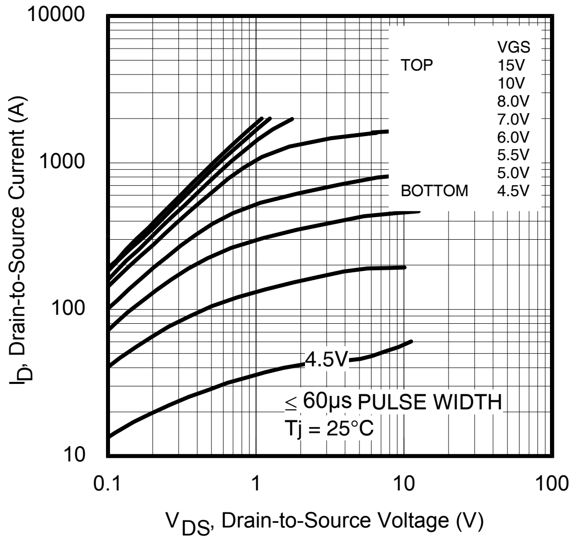



**Fig. 1** Typical Output Characteristics

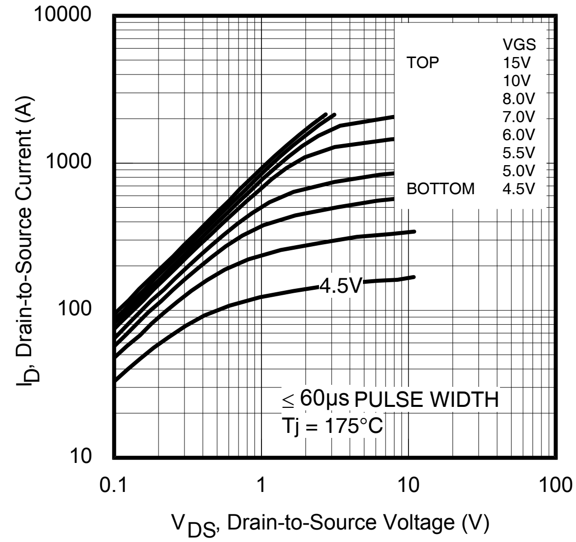



**Fig. 2** Typical Output Characteristics

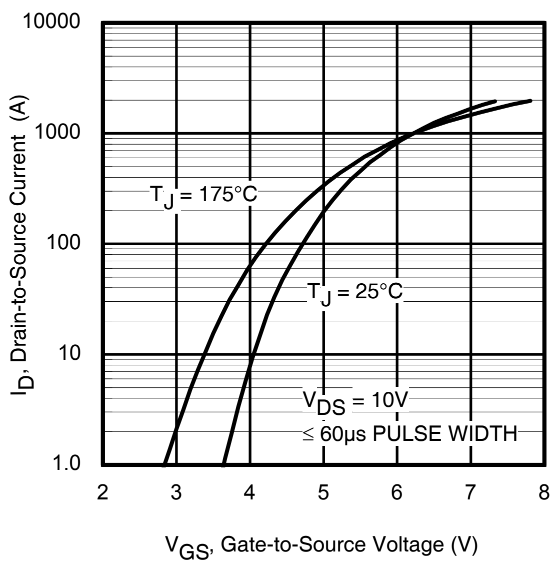



**Fig. 3** Typical Transfer Characteristics

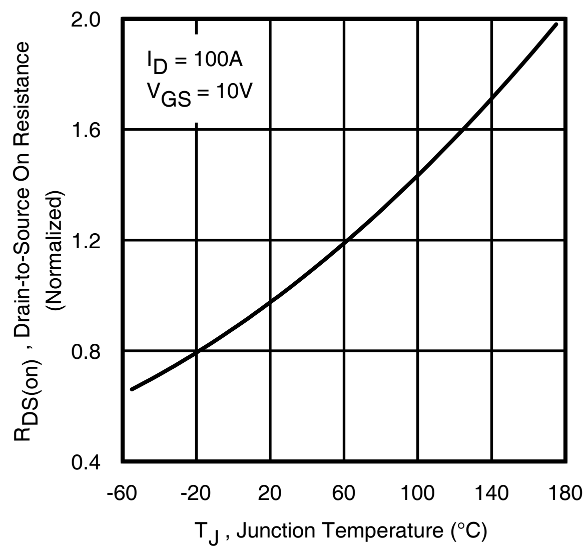



**Fig. 4** Normalized On-Resistance vs. Temperature

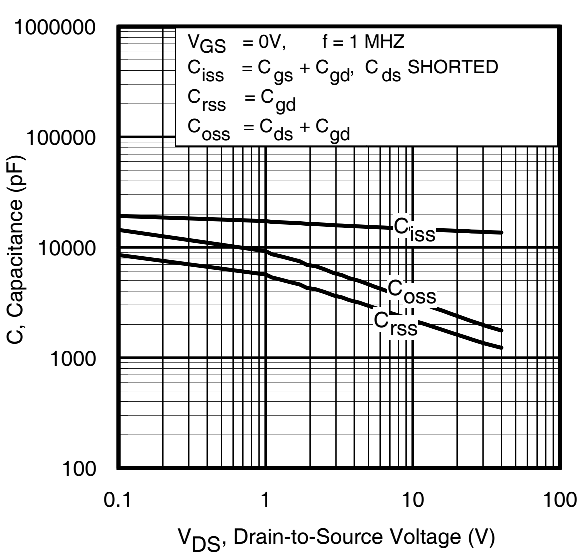



**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage

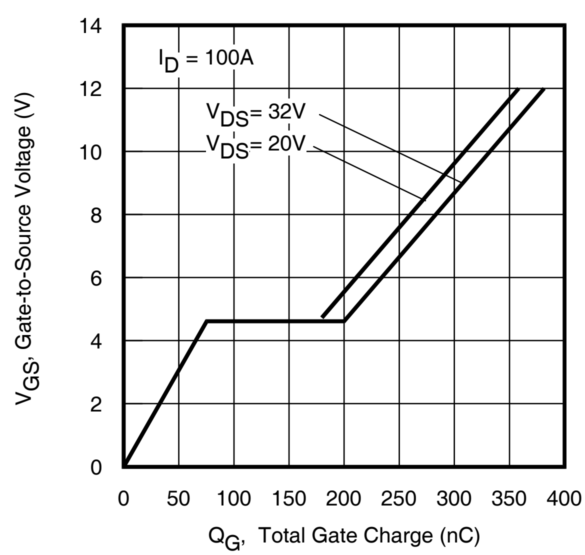



**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage

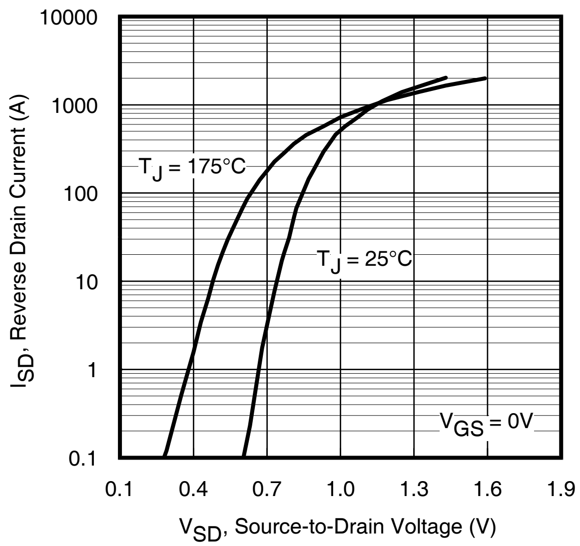



**Fig. 7** Typical Source-to-Drain Diode Forward Voltage

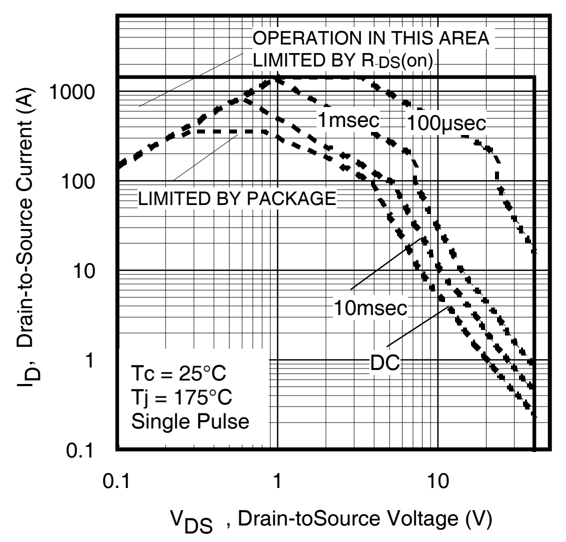



**Fig 8.** Maximum Safe Operating Area

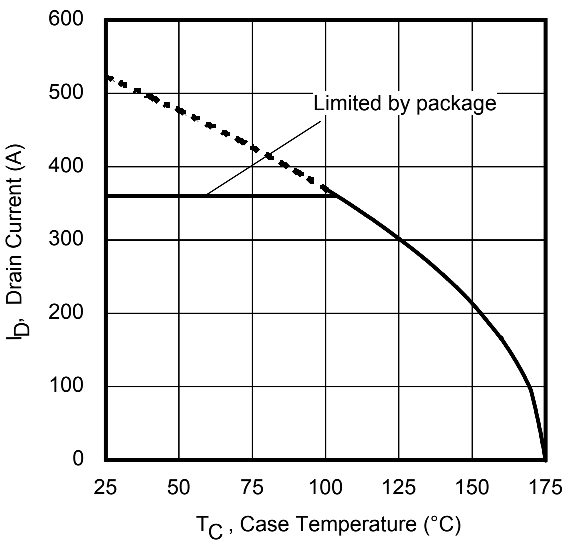



**Fig 9.** Maximum Drain Current vs. Case Temperature

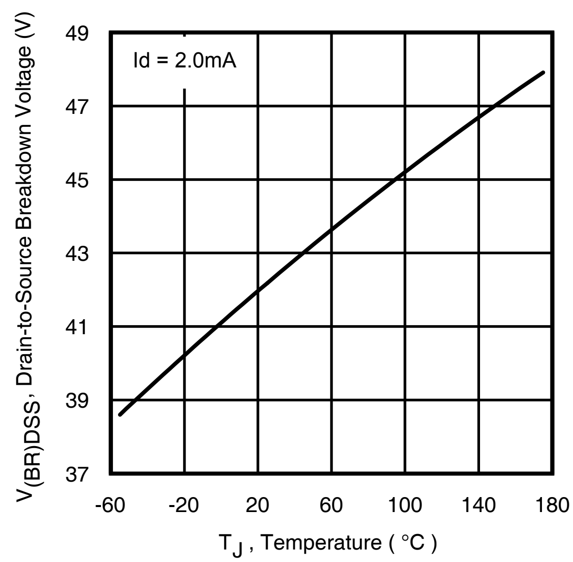



**Fig 10.** Drain-to-Source Breakdown Voltage

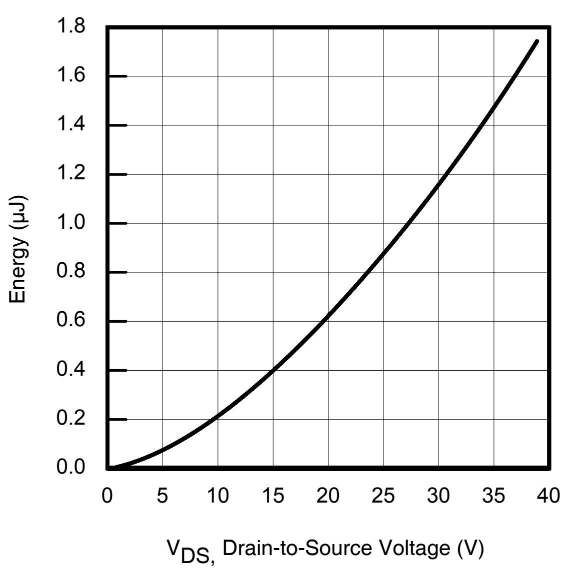



**Fig 11.** Typical Coss Stored Energy

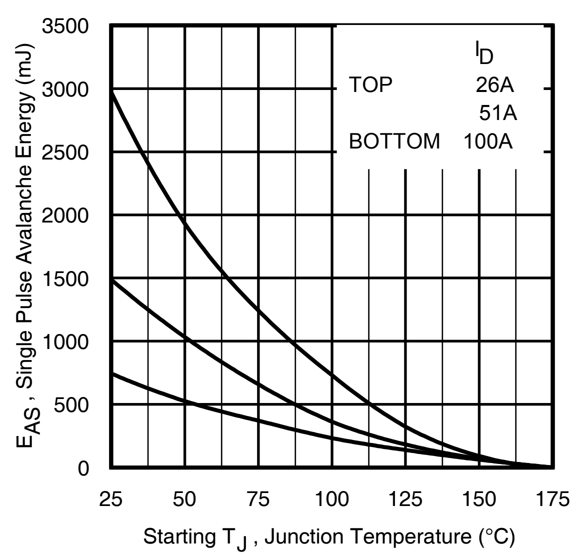



**Fig 12.** Maximum Avalanche Energy vs. Drain Current

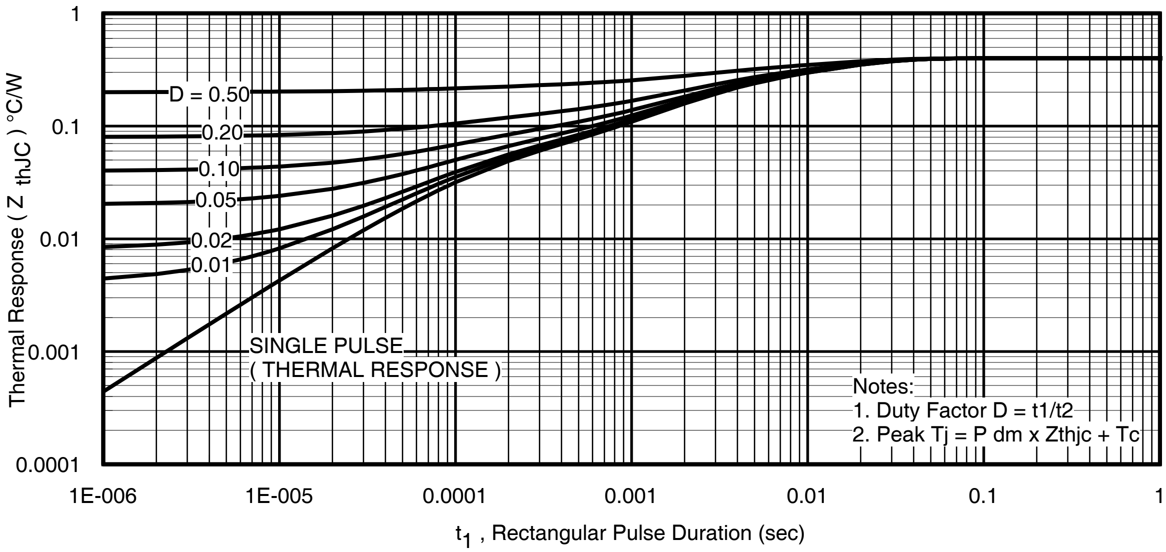



**Fig 13.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

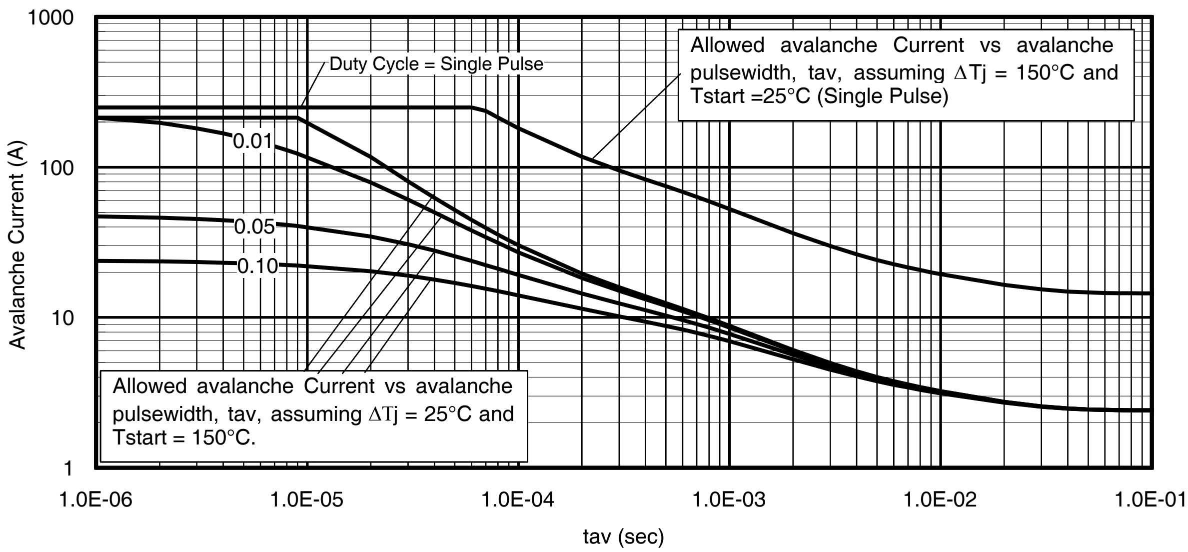



**Fig 14.** Avalanche Current vs. Pulse width

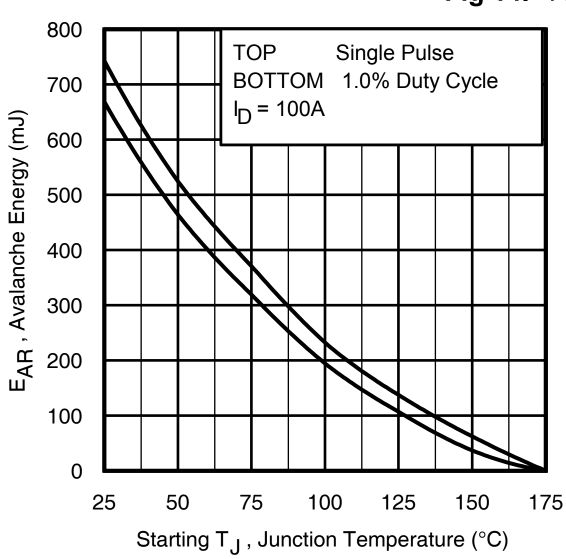



**Fig 15.** Maximum Avalanche Energy vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 14, 15:**
**(For further info, see AN-1005 at www.irf.com)**

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of $T_{jmax}$. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as $T_{jmax}$ is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 24a, 24b.
4. $P_{D\,(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. $I_{av}$ = Allowable avalanche current.
7. $\Delta T$ = Allowable rise in junction temperature, not to exceed $T_{jmax}$ (assumed as 25°C in Figure 13, 14).
   $t_{av}$ = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13.

$$P_{D\,(ave)} = 1/2\ (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
$$E_{AS\,(AR)} = P_{D\,(ave)} \cdot t_{av}$$

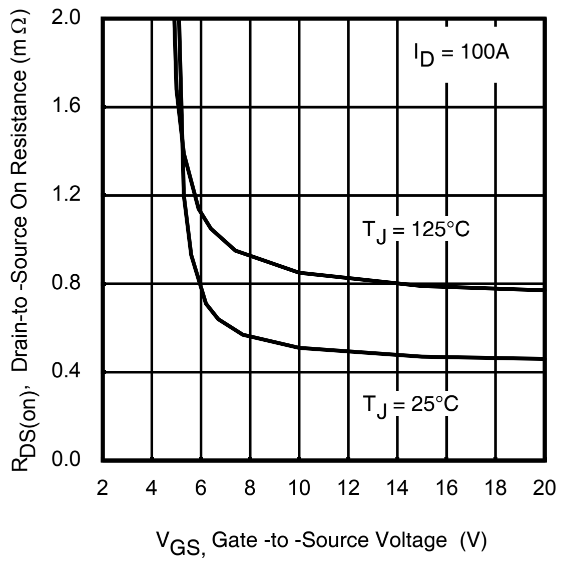



**Fig 16.** Typical On-Resistance vs. Gate Voltage

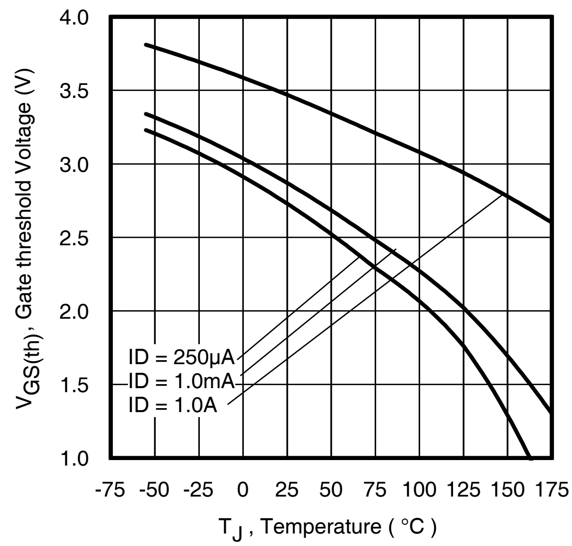



**Fig 17.** Threshold Voltage vs. Temperature

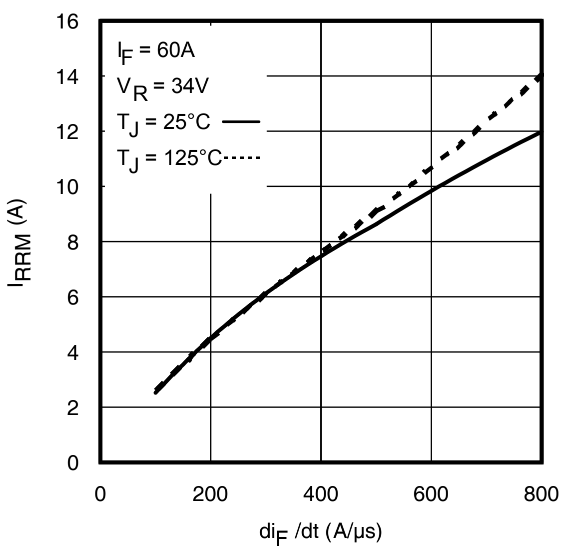



**Fig. 18** - Typical Recovery Current vs. dif/dt

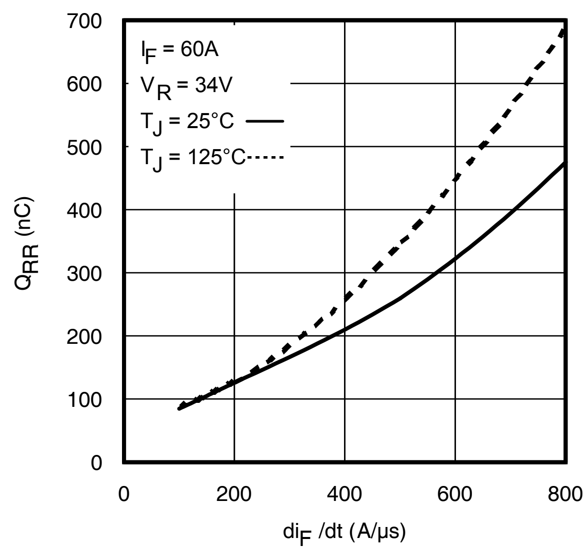



**Fig. 19** - Typical Stored Charge vs. dif/dt

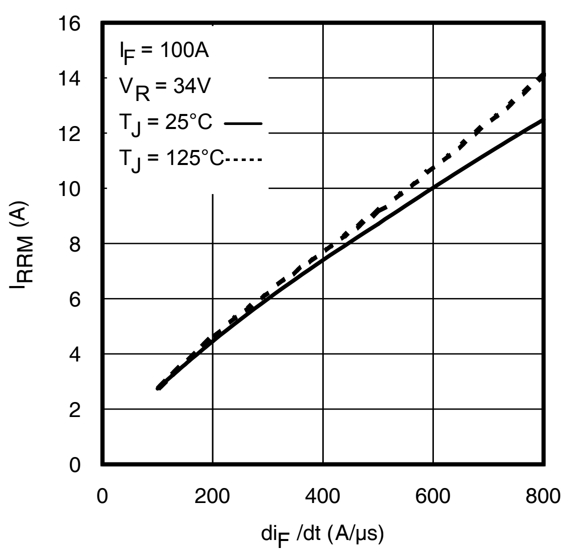



**Fig. 20** - Typical Recovery Current vs. dif/dt

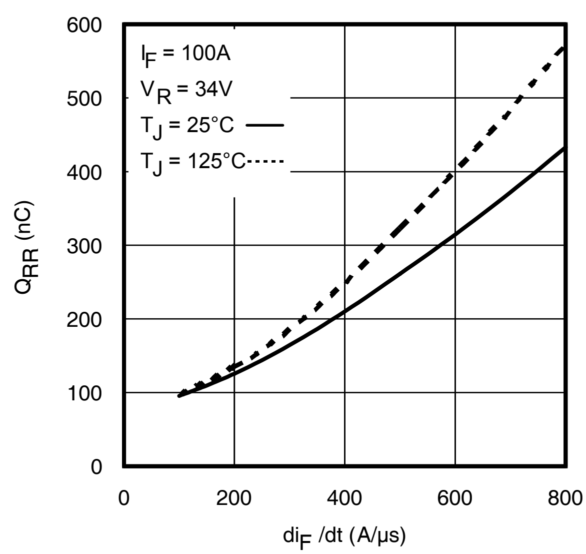



**Fig. 21** - Typical Stored Charge vs. dif/dt

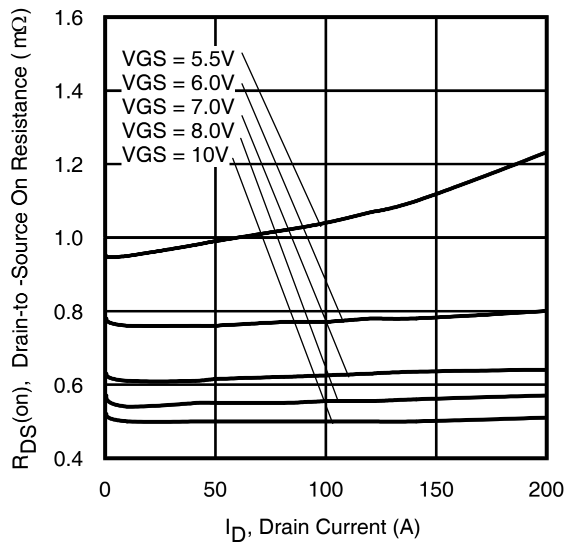



**Fig 22.** Typical On-Resistance vs. Drain Current

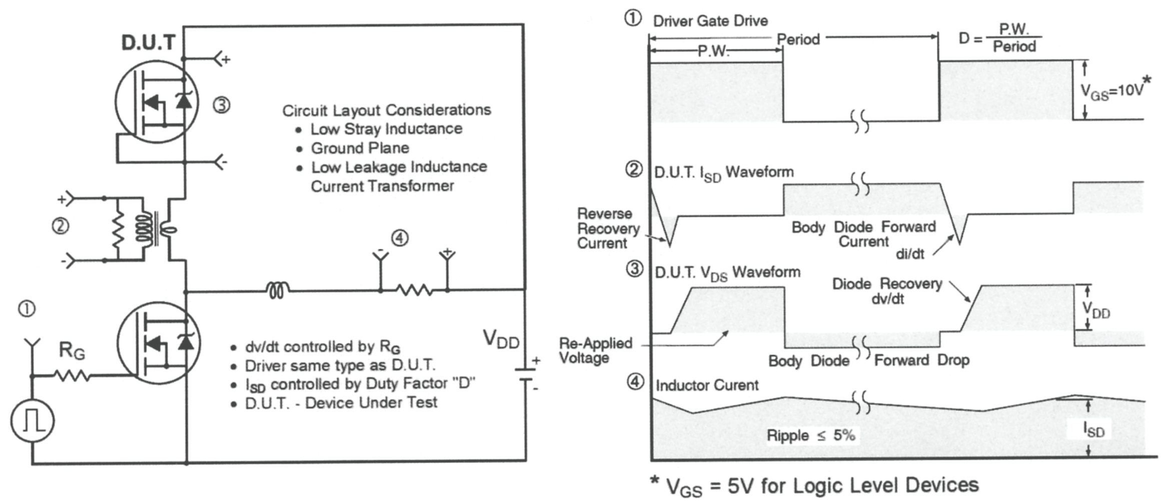



**Fig 23.** Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

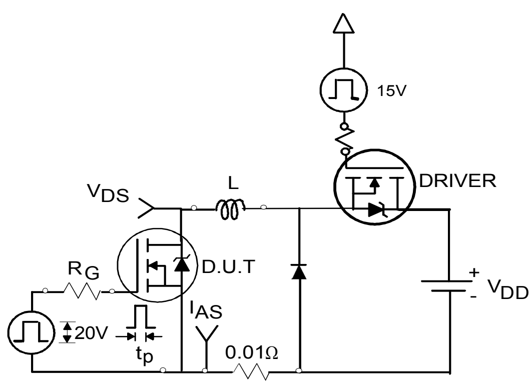



**Fig 24a.** Unclamped Inductive Test Circuit

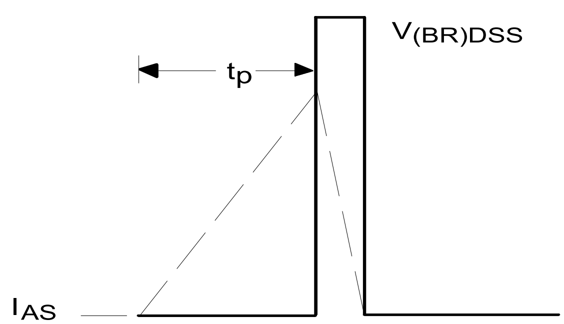



**Fig 24b.** Unclamped Inductive Waveforms

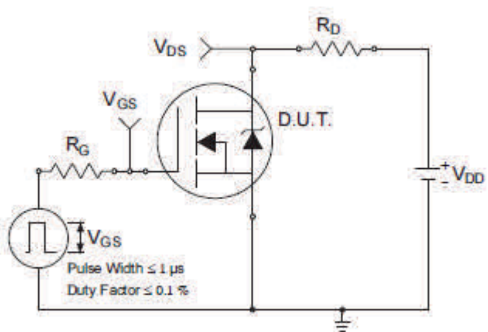



**Fig 25a.** Switching Time Test Circuit

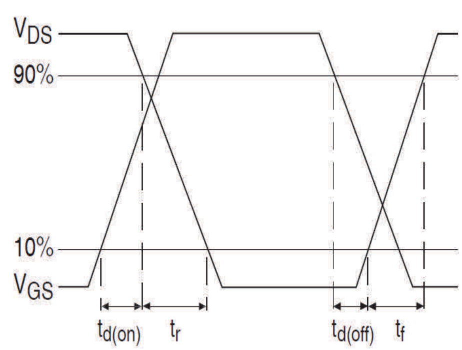



**Fig 25b.** Switching Time Waveforms

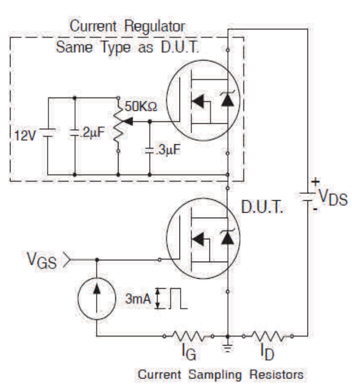



**Fig 26a.** Gate Charge Test Circuit

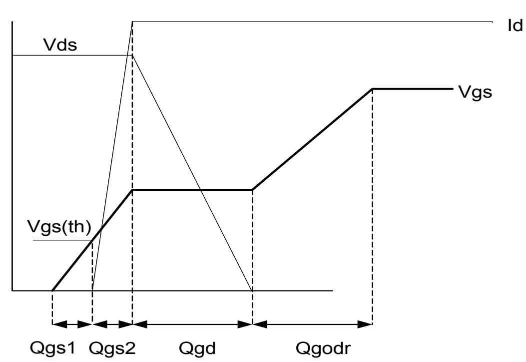
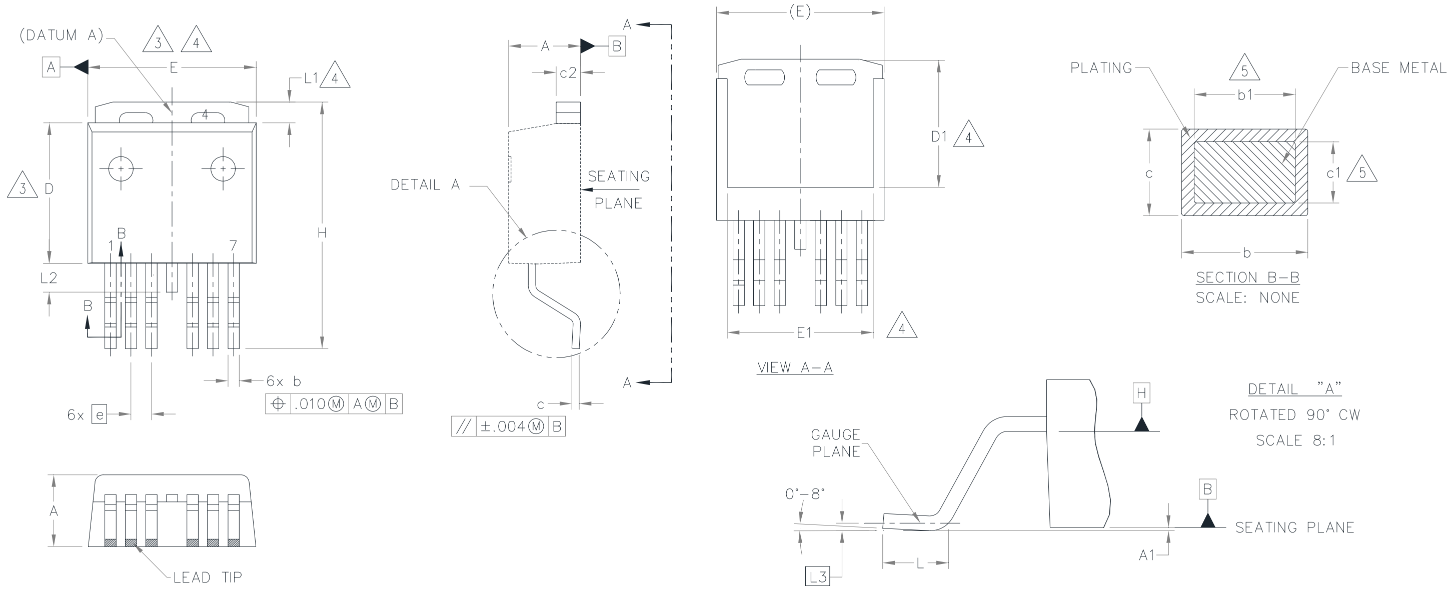



**Fig 26b.** Gate Charge Waveform

## $D^2$PAK-7TP Package Outline (Dimensions are shown in millimeters (inches))



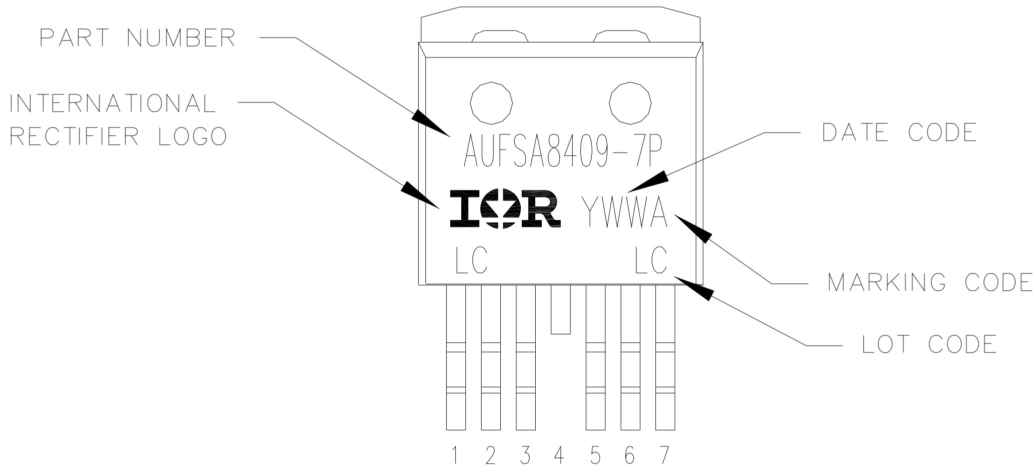

| SYMBOL | DIMENSIONS | | | | NOTES |
|---|---|---|---|---|---|
| | MILLIMETERS | | INCHES | | |
| | MIN. | MAX. | MIN. | MAX. | |
| A | 4.06 | 4.83 | .160 | .190 | |
| A1 | – | 0.254 | – | .010 | |
| b | 0.51 | 0.91 | .020 | .036 | |
| b1 | 0.51 | 0.81 | .020 | .032 | 5 |
| c | 0.38 | 0.74 | .015 | .029 | |
| c1 | 0.38 | 0.58 | .015 | .023 | 5 |
| c2 | 1.14 | 1.65 | .045 | .065 | |
| D | 8.38 | 9.65 | .330 | .380 | 3 |
| D1 | 6.86 | 7.42 | .270 | .292 | 4 |
| E | 9.65 | 10.54 | .380 | .415 | 3,4 |
| E1 | 8.00 | 9.00 | .315 | .354 | 4 |
| e | 1.27 BSC | | .050 BSC | | |
| H | 14.61 | 15.88 | .575 | .625 | |
| L | 1.78 | 2.79 | .070 | .110 | |
| L1 | – | 1.68 | – | .066 | 4 |
| L2 | – | 1.78 | – | .070 | |
| L3 | 0.25 BSC | | .010 BSC | | |

NOTES:

1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M–1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263CB. EXCEPT FOR DIMS. E, E1 & D1.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

## D[2]PAK-7TP Part Marking Information

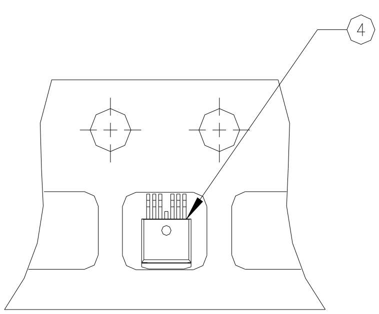


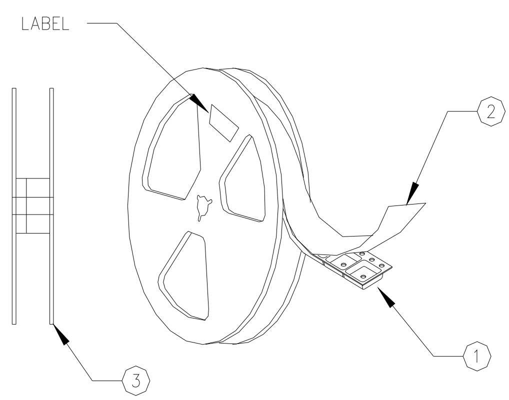

## D[2]PAK-7TP Tape and Reel

NOTES, TAPE & REEL, LABELLING:

1. TAPE AND REEL.
   - 1.1 REEL SIZE 13 INCH DIAMETER.
   - 1.2 EACH REEL CONTAINING 800 DEVICES.
   - 1.3 THERE SHALL BE A MINIMUM OF 42 SEALED POCKETS CONTAINED IN THE LEADER AND A MINIMUM OF 15 SEALED POCKETS IN THE TRAILER.
   - 1.4 PEEL STRENGTH MUST CONFORM TO THE SPEC. NO. 71-9667.
   - 1.5 PART ORIENTATION SHALL BE AS SHOWN BELOW.
   - 1.6 REEL MAY CONTAIN A MAXIMUM OF TWO UNIQUE LOT CODE/DATE CODE COMBINATIONS. REWORKED REELS MAY CONTAIN A MAXIMUM OF THREE UNIQUE LOT CODE/DATE CODE COMBINATIONS. HOWEVER, THE LOT CODES AND DATE CODES WITH THEIR RESPECTIVE QUANTITIES SHALL APPEAR ON THE BAR CODE LABEL FOR THE AFFECTED REEL.

2. LABELLING (REEL AND SHIPPING BAG).
   - 2.1 CUST. PART NUMBER (BAR CODE): IRFXXXXSTRL-7P
   - 2.2 CUST. PART NUMBER (TEXT CODE): IRFXXXXSTRL-7P
   - 2.3 I.R. PART NUMBER: IRFXXXXSTRL-7P
   - 2.4 QUANTITY:
   - 2.5 VENDOR CODE: IR
   - 2.6 LOT CODE:
   - 2.7 DATE CODE:




Note: For the most current drawing please refer to IR website at [http://www.irf.com/package/](http://www.irf.com/package/)

**Qualification Information†**

| | | | |
|---|---|---|---|
| **Qualification Level** | | Automotive (per AEC-Q101) | |
| | | Comments: This part number(s) passed Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level. | |
| | | $D^2$PAK-7TP | MSL1 |
| **ESD** | Human Body Model | Class H3A (± 8000V) † AEC-Q101-001 | |
| | Charged Device Model | Class C5 (± 2000V) † AEC-Q101-005 | |
| **RoHS Compliant** | | Yes | |

† Highest passing voltage.

**Published by**
**Infineon Technologies AG**
**81726 München, Germany**