



MOSFET

OptiMOS[™]3 Power MOS Transistor Chip

- N-channel enhancement mode
- · For dynamic characterization refer to the datasheet of IPB011N04N G
- AQL 0.65 for visual inspection according to failure catalogue
- Electrostatic Discharge Sensitive Device according to MIL-STD 883C
- Die bond: soldered or glued
- Backside metallization: NiV system
- Frontside metallization: AICu system
- Passivation: Nitride + Imide

Table 1Key Performance Parameters

Parameter	Value	Unit
V _{(BR)DSS}	40	V
R _{DS(on)}	1.1 ¹⁾	mΩ
Die size	5.9 x 3.7	mm ²
Thickness	175	μm









Type / Ordering Code	Package	Marking	Related Links
IPC218N04N3	Chip	not defined	-

1 Electrical Characteristics on Wafer Level

at $T_j = 25^{\circ}$ C, unless otherwise specified

Table 2

Devenuenter	Symbol		Values		11	Note / Test Condition
Parameter		Min.	Тур.	Max.	Unit	Note / Test Condition
Drain-source breakdown voltage	V _{(BR)DSS}	40	-	-	V	V _{GS} =0 V , <i>I</i> _D =1 mA
Gate threshold voltage	V _{GS(th)}	2	-	4	V	<i>V</i> _{DS} = <i>V</i> _{GS} , <i>I</i> _D =200 μA
Zero gate voltage drain current	I _{DSS}	-	0.1	2	μA	V _{GS} =0 V ,V _{DS} =40 V
Gate-source leakage current	I _{GSS}	-	2	200	nA	V _{GS} =20 V , V _{DS} =0 V
Drain-source on- resistance	R _{DS(on)}	-	0.9 ²⁾	50 ³⁾	mΩ	V _{GS} =10 V , <i>I</i> _D =2.0 A
Reverse diode forward on-voltage	V _{SD}	-	0.86	1.1	V	V _{GS} =0 V , <i>I</i> _F =1A
Internal gate resistance	R _G	-	1.5	-	Ω	-
Avalanche energy, single pulse	E _{AS}	-	-	525 ⁴⁾	mJ	I _D =50 A, R _{GS} =25 Ω

¹⁾ packaged in a PG-TO263-7 (see ref. product)

³⁾ limited by wafer test-equipment

²⁾ typical bare die $R_{DS(on)}$; V_{GS} =10 V when used with 4*500µm Al-wedge double-stitch bonding

⁴⁾ Wafer tested. For general avalanche capability refer to the datasheet of IPB011N04N G

2 Package Outlines







Revision History

IPC218N04N3

Revision: 2017-07-17, Rev. 2.6

Previous Revision					
Revision	Date	e Subjects (major changes since last revision)			
2.5	2014-07-25	Release Final Version			
2.6	2017-07-17	Change typical RDS(on)			

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