

TDM Microphone Array Demo Board Guide

GENERAL DESCRIPTION

This user guide describes operation of the TDM Microphone Array Demo board, which uses 16 ICS-52000 microphones.

This allows evaluation of the ICS-52000 in a large 4x4 array, with 15 mm spacing between adjacent microphones in the array. The order of the microphones in the 16 TDM slots in shown on the board's top silkscreen.

TABLE 1. BOARD SETTINGS

Headers, Jumpers, Switches	Description
J1	TDM data interface
J2	Connect SCK to mics 1-4
J3	Connect SCK to mics 5-8
J4	Connect SCK to mics 9-12
J5	Connect SCK to mics 13-16
J6	Connect SD between rows 1 & 2
J7	Connect SD between rows 2 & 3
J8	Connect SD between rows 3 & 4
J9	Board power connection, >2.3 V, 40 mA
S1	Select whether the board's SD output signal is buffered (left) or unbuffered (right).
S2	Select whether the board's SCK input signal is buffered (left) or unbuffered (right)

TABLE 2. J1 PINOUT

Pin	Function
1	Board VDD, Output of 1.8 V regulator. Do not connect external supply to this pin.
3	No connect
5	SD – microphone data output
7	SCK – microphone serial clock input
9	WS – microphone frame clock input
2, 4, 6, 8, 10	Ground

BOARD OPERATION

The board can be set up for arrays of 4, 8, 12, or 16 microphones. The SCK signal to each horizontal row of four microphones is enabled with jumpers J2-5. For an array of 4 mics, only populate jumper J2, for an array of 8 mics, populate J2 & J3, and so on.

Jumpers J6-8 are used to connect or disconnect the SD trace between rows, depending on how many mics are being used. This is to minimize the loading of the SD line on a long trace.

Typically, switches S1 and S2 are set to enable buffers for the SD output and SCK input. These can be disabled if necessary for evaluation.

The board is powered by applying 2.3 - 3.3 V on J9. The bottom pin of this jumper is VDD, the top pin is ground.

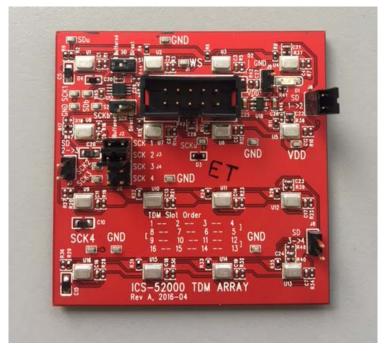


Figure 1. TDM Microphone Array Demo Board

InvenSense reserves the right to change the detail specifications as may be required to permit improvements in the design of its products.

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SCHEMATIC

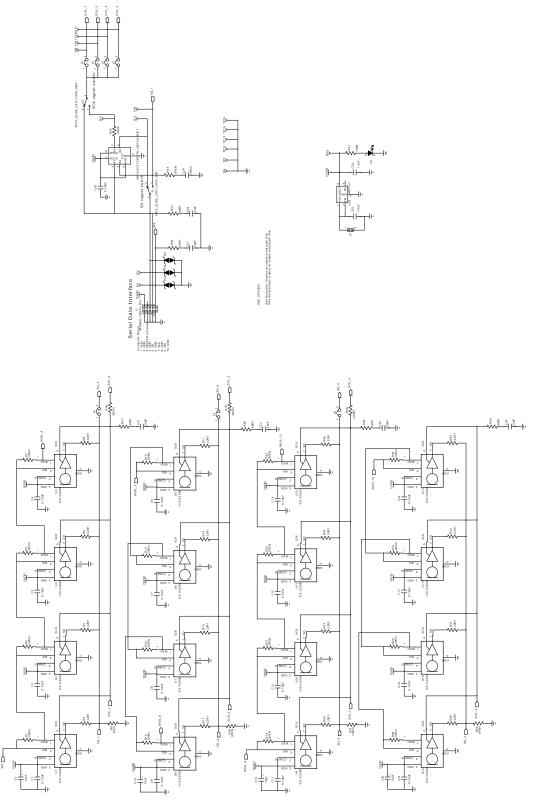


Figure 2. Schematic



REVISION HISTORY

Revision Date	Revision	Description
4/6/2017	1.0	Initial Release



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