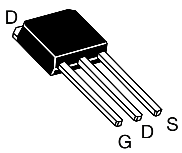
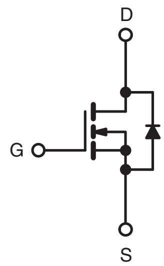
D Series Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	550	
$R_{DS(on)}$ max. at 25 °C (Ω)	V_{GS} = 10 V	3.2
Q_g (max.) (nC)	12	
Q_{gs} (nC)	2	
Q_{gd} (nC)	3	
Configuration	Single	

IPAK
(TO-251)





N-Channel MOSFET

FEATURES

- Optimal design
  - Low area specific on-resistance
  - Low input capacitance (C_{iss})
  - Reduced capacitive switching losses
  - High body diode ruggedness
  - Avalanche energy rated (UIS)
- Optimal efficiency and operation
  - Low cost
  - Simple gate drive circuitry
  - Low figure-of-merit (FOM): R_{on} x Q_g
  - Fast switching
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Consumer electronics
  - Displays (LCD or plasma TV)
- Server and telecom power supplies
  - SMPS
- Industrial
  - Welding, induction heating, motor drives
- Battery chargers

ORDERING INFORMATION	
Package	IPAK (TO-251)
Lead (Pb)-free and Halogen-free	SiHU3N50DA-GE3

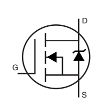
ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	500	V
Gate-Source Voltage			V_{GS}	± 30	
Gate-Source Voltage AC (f > 1 Hz)				30	
Continuous Drain Current (T_J = 150 °C)	V_{GS} at 10 V	T_C = 25 °C	I_D	3.0	A
		T_C = 100 °C		1.9	
Pulsed Drain Current[a]			I_{DM}	5.5	
Linear Derating Factor				0.56	W/°C
Single Pulse Avalanche Energy[b]			E_{AS}	9	mJ
Maximum Power Dissipation			P_D	69	W
Operating Junction and Storage Temperature Range			T_J, T_{stg}	-55 to +150	°C
Drain-Source Voltage Slope	T_J = 125 °C		dV/dt	24	V/ns
Reverse Diode dV/dt[d]				0.22	
Soldering Recommendations (Peak Temperature)[c]	for 10 s			300	°C

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature.
b. V_{DD} = 50 V, starting T_J = 25 °C, L = 2.3 mH, R_g = 25 Ω, I_{AS} = 2.8 A.
c. 1.6 mm from case.
d. $I_{SD} \leq I_D$, starting T_J = 25 °C.

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.8	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA		500	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA		-	0.59	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA		3	-	4.5	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 30 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 500 V, V_{GS} = 0 V		-	-	1	μA
		V_{DS} = 400 V, V_{GS} = 0 V, T_J = 125 °C		-	-	10	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 1.5 A	-	2.6	3.2	Ω
Forward Transconductance	g_{fs}	V_{DS} = 8 V, I_D = 1.5 A		-	1	-	S
Dynamic							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz		-	177	-	pF
Output Capacitance	C_{oss}			-	26	-	
Reverse Transfer Capacitance	C_{rss}			-	7	-	
Effective Output Capacitance, Energy Related[b]	$C_{o(er)}$	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		-	21	-	
Effective Output Capacitance, Time Related[c]	$C_{o(tr)}$			-	28	-	
Total Gate Charge	Q_g	V_{GS} = 10 V	I_D = 1.5 A, V_{DS} = 400 V	-	6	12	nC
Gate-Source Charge	Q_{gs}			-	2	-	
Gate-Drain Charge	Q_{gd}			-	3	-	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 400 V, I_D = 1.5 A, R_g = 9.1 Ω, V_{GS} = 10 V		-	12	24	ns
Rise Time	t_r			-	9	18	
Turn-Off Delay Time	$t_{d(off)}$			-	11	22	
Fall Time	t_f			-	13	26	
Gate Input Resistance	R_g	f = 1 MHz, open drain		-	2.6	-	Ω
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse P - N junction diode 		-	-	3	A
Pulsed Diode Forward Current	I_{SM}			-	-	5.5	
Diode Forward Voltage	V_{SD}	T_J = 25 °C, I_S = 1.5 A, V_{GS} = 0 V		-	-	1.2	V
Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = I_S = 1.5 A, dI/dt = 100 A/μs, V_R = 25 V		-	285	570	ns
Reverse Recovery Charge	Q_{rr}			-	0.68	1.36	μC
Reverse Recovery Current	I_{RRM}			-	5	-	A

Notes

a. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}.
b. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

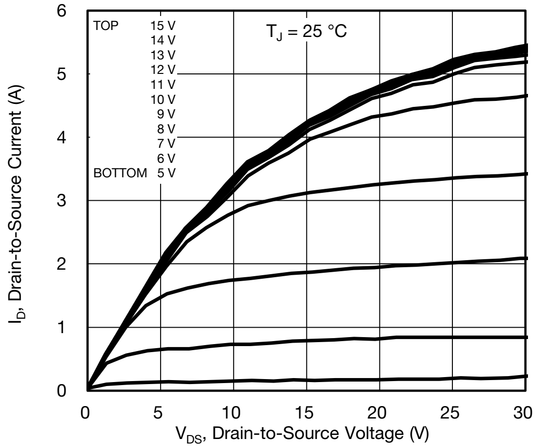


Fig. 1 - Typical Output Characteristics

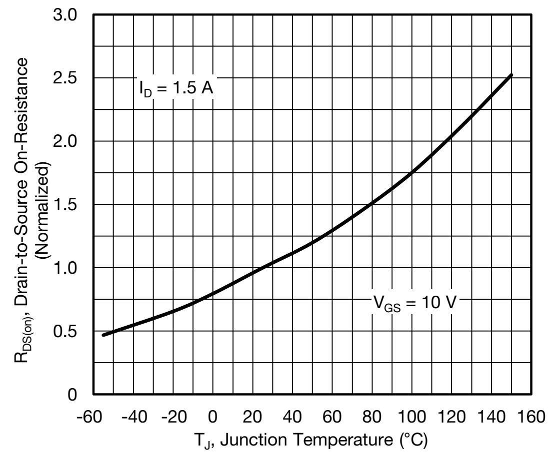


Fig. 4 - Normalized On-Resistance vs. Temperature

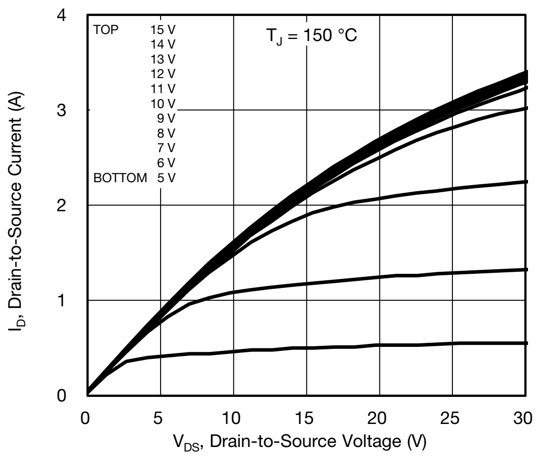


Fig. 2 - Typical Output Characteristics

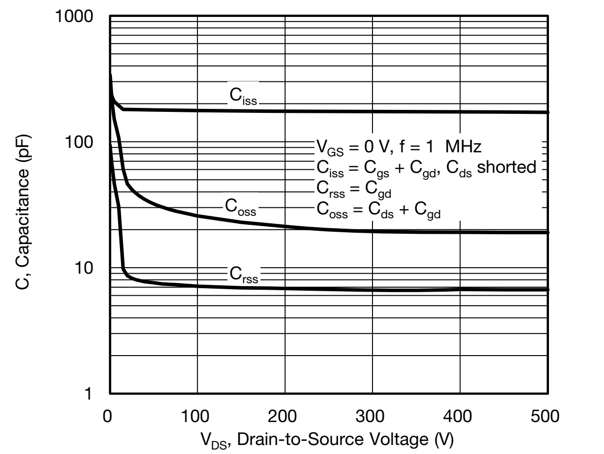


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

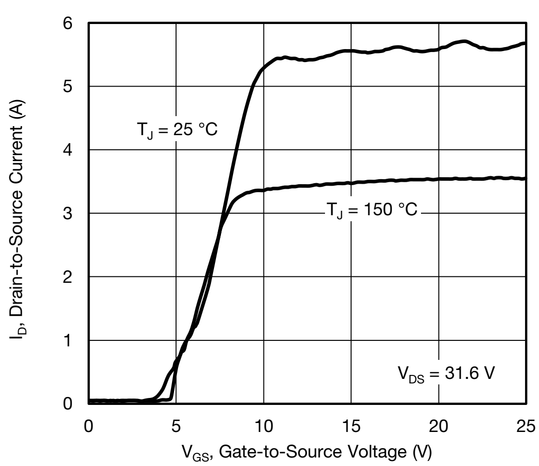


Fig. 3 - Typical Transfer Characteristics

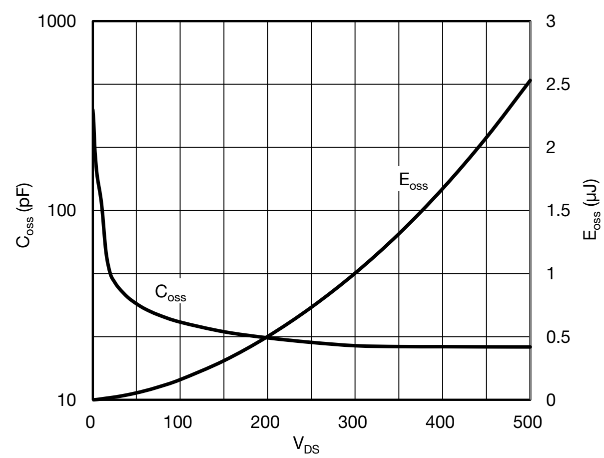


Fig. 6 - C_{oss} and E_{oss} vs. V_{DS}

For technical questions, contact: hvm@vishay.com

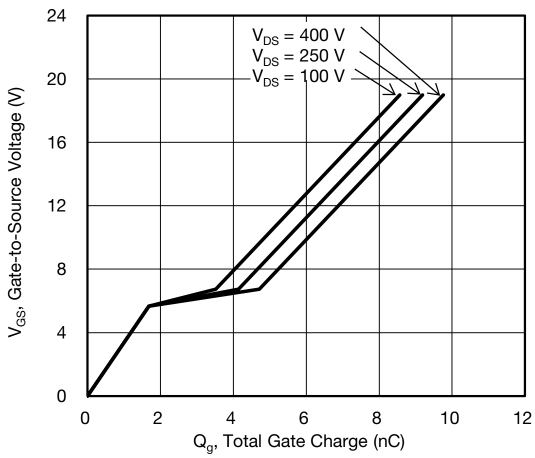


Fig. 7 - Typical Gate Charge vs. Gate-to-Source Voltage

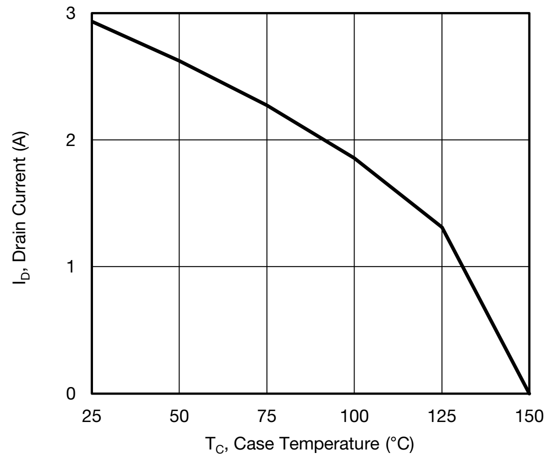


Fig. 10 - Maximum Drain Current vs. Case Temperature

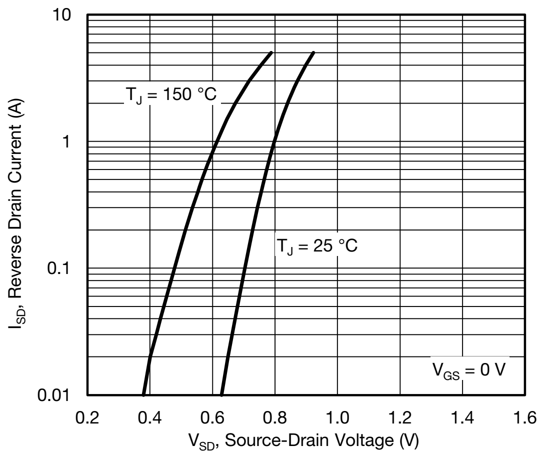


Fig. 8 - Typical Source-Drain Diode Forward Voltage

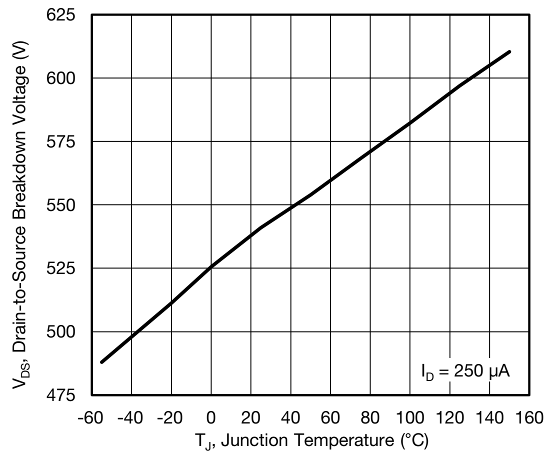
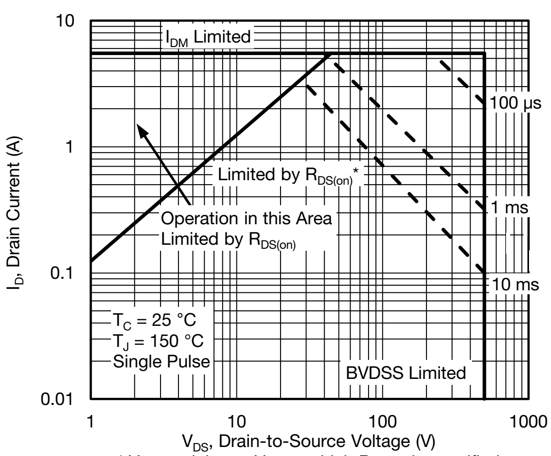


Fig. 11 - Typical Drain-to-Source Voltage vs. Temperature



* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Fig. 9 - Maximum Safe Operating Area

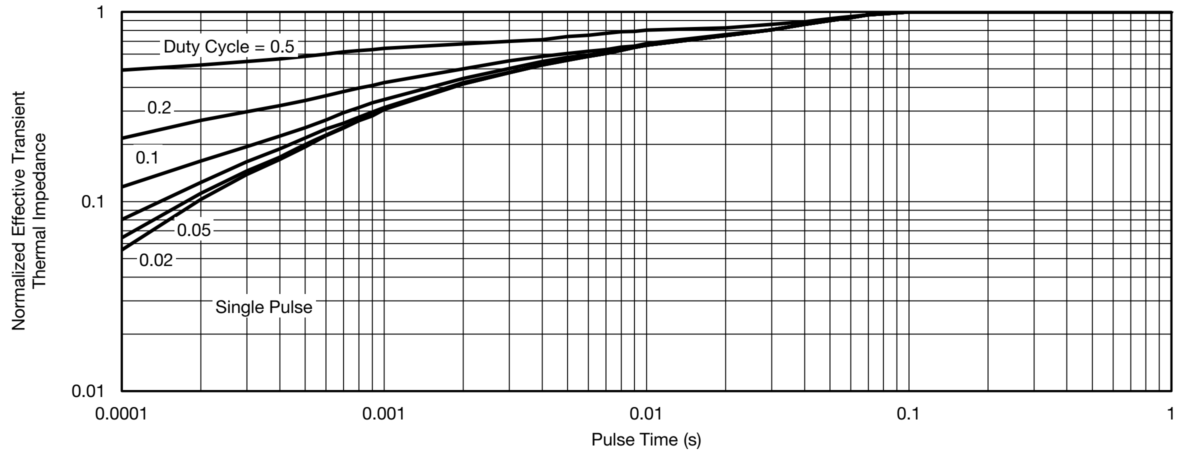


Fig. 12 - Normalized Thermal Transient Impedance, Junction-to-Case

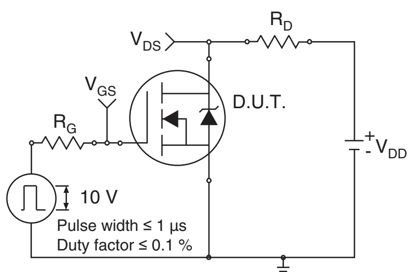


Fig. 13 - Switching Time Test Circuit

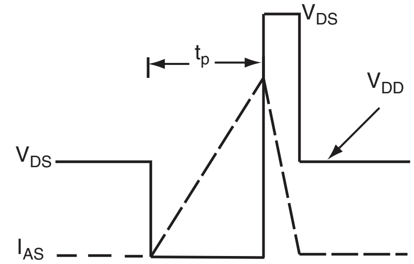


Fig. 16 - Unclamped Inductive Waveforms

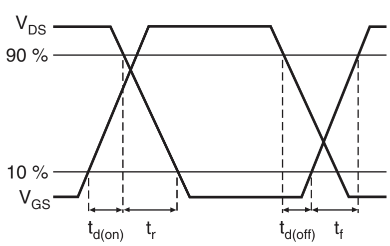


Fig. 14 - Switching Time Waveforms

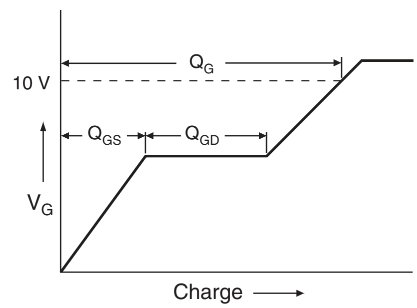


Fig. 17 - Basic Gate Charge Waveform

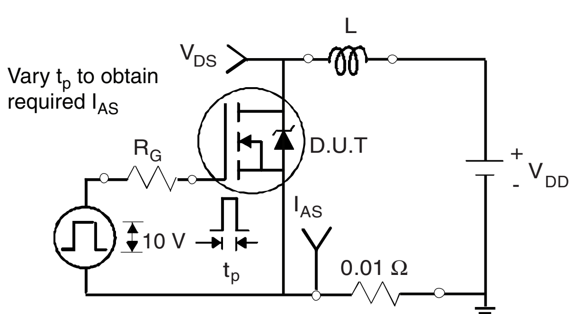


Fig. 15 - Unclamped Inductive Test Circuit

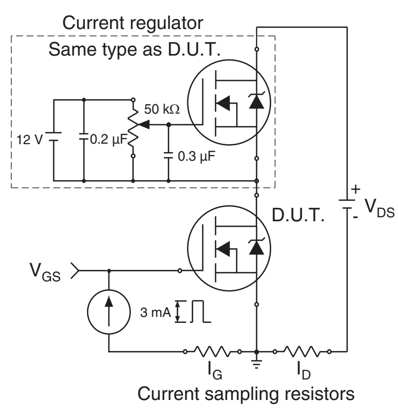
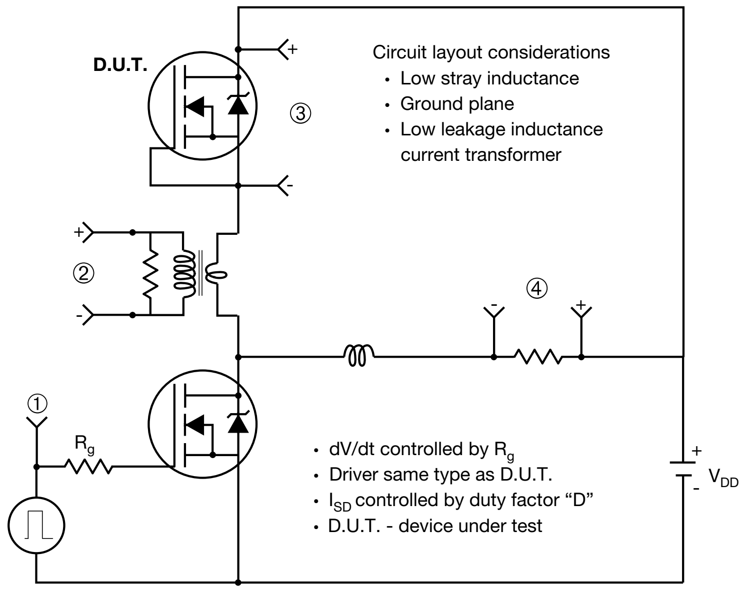
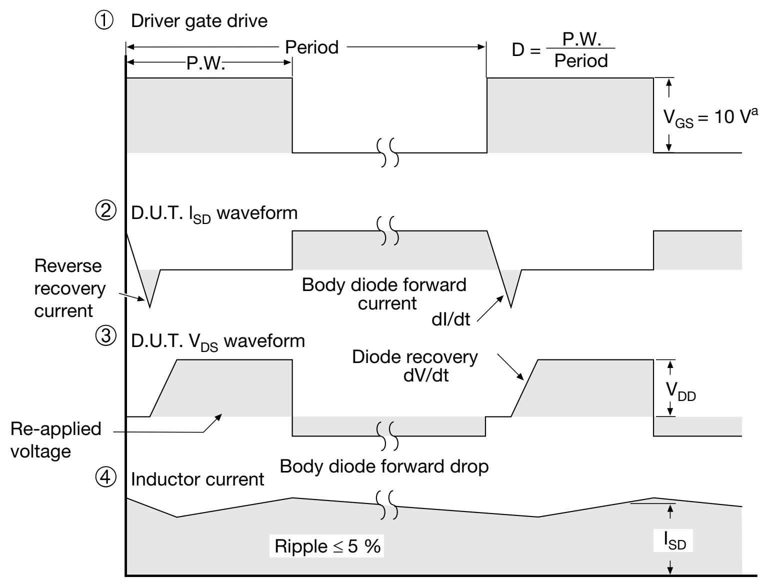


Fig. 18 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit





Note

a. V_{GS} = 5 V for logic level devices

Fig. 19 - For N-Channel

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