AUTOMOTIVE GRADE

International

- Advanced Process Technology
- Ultra Low On-Resistance
- 50% Lower Lead Resistance
- 175°C Operating Temperature
- Fast Switching

Features

- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free, RoHS Compliant
- Automotive Qualified *

Description

Specifically design for automotive applications this Widelead TO-262 package part has the advantage of having over 50% lower lead resistance and delivering over 20% lower Rds(on) when compared with a traditional TO-262 package housing the same silicon die. This greatly helps in reducing condition losses, achieving higher current levels or enabling a system to run cooler and have improved efficiency. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive and other applications.

AUIRF3004WL

WIDELEAD HEXFET® Power MOSFET



V _{(BR)DSS}	40V
R _{DS(on)} typ.	1.27m Ω
max.	1.40m Ω
LD (Silicon Limited)	386A ①
D (Package Limited)	240A



G	D	S
Gate	Drain	Source

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (T_A) is 25°C, unless otherwise specified.

	Parameter	Max.	Units
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V (Silicon Limited)	386 ①	
$I_{\rm D} @ T_{\rm C} = 100^{\circ}{\rm C}$	Continuous Drain Current, V _{GS} @ 10V (Silicon Limited)	273①	
$I_{\rm D} @ T_{\rm C} = 25^{\circ}{\rm C}$	Continuous Drain Current, V _{GS} @ 10V (Package Limited)	240	
I _{DM}	Pulsed Drain Current 2	1544	
$P_{D} @ T_{C} = 25^{\circ}C$	Maximum Power Dissipation	375	W
	Linear Derating Factor	2.5	W/°C
V _{GS}	Gate-to-Source Voltage	± 20	V
EAS (Thermally limited)	Single Pulse Avalanche Energy 3	470	mJ
I _{AR}	Avalanche Current 2	See Fig. 14, 15, 22a, 22b,	A
E _{AR}	Repetitive Avalanche Energy ©		mJ
dv/dt	Peak Diode Recovery ④	6.1	V/ns
TJ	Operating Junction and	-55 to + 175	
T _{STG}	Storage Temperature Range		°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

	Parameter	Тур.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ®		0.40	°C/W

 $\mathsf{HEXFET}^{\texttt{R}}$ is a registered trademark of International Rectifier.

*Qualification standards can be found at http://www.irf.com/

Static Electrical Characteristics @ T_{.1} = 25°C (unless otherwise specified)

	Parameter	Min.	Тур.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	40			V	$V_{GS} = 0V, I_{D} = 250\mu A$
$\Delta V_{(BR)DSS} / \Delta T_J$	Breakdown Voltage Temp. Coefficient		0.038		V/°C	Reference to 25°C, I _D = 5mA ⑤
R _{DS(on)}	Static Drain-to-Source On-Resistance		1.27	1.40	mΩ	V _{GS} = 10V, I _D = 195A
V _{GS(th)}	Gate Threshold Voltage	2.0		4.0	V	$V_{DS} = V_{GS}$, $I_D = 250 \mu A$
gfs	Forward Transconductance	330			S	V _{DS} = 10V, I _D = 195A
R _G	Internal Gate Resistance		2.7		Ω	
I _{DSS}	Drain-to-Source Leakage Current			20		$V_{DS} = 40V, V_{GS} = 0V$
				250	μA	$V_{DS} = 32V, V_{GS} = 0V, T_{J} = 125^{\circ}C$
I _{GSS}	Gate-to-Source Forward Leakage			100	۳Å	V _{GS} = 20V
	Gate-to-Source Reverse Leakage			-100	nA	V _{GS} = -20V

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Тур.	Max.	Units	Conditions
Q _g	Total Gate Charge		140	210		I _D = 232A
Q _{gs}	Gate-to-Source Charge		53		nC	V _{DS} =20V
Q _{gd}	Gate-to-Drain ("Miller") Charge		49			V _{GS} = 10V ⑤
Q _{sync}	Total Gate Charge Sync. (Q _g - Q _{gd})		91			$I_{D} = 232A, V_{DS} = 0V, V_{GS} = 10V$ (5)
t _{d(on)}	Turn-On Delay Time		19			$V_{DD} = 26V$
t _r	Rise Time		220			I _D = 232A
t _{d(off)}	Turn-Off Delay Time		90		ns	$R_{G} = 2.7\Omega$
t _f	Fall Time		130			V _{GS} = 10V ⑤
C _{iss}	Input Capacitance		9450			V _{GS} = 0V
C _{oss}	Output Capacitance		1930			$V_{DS} = 32V$
C _{rss}	Reverse Transfer Capacitance		975		pF	f = 1.0MHz, See Fig.5
C _{oss} eff. (ER)	Effective Output Capacitance (Energy Related)		2330			$V_{GS} = 0V, V_{DS} = 0V$ to 32V \odot , See Fig.11
C _{oss} eff. (TR)	Effective Output Capacitance (Time Related)		2815			$V_{GS} = 0V, V_{DS} = 0V \text{ to } 32V \text{ (6)}$

Diode Characteristics

	Parameter	Min.	Тур.	Max.	Units	Conditions
I _s	Continuous Source Current			386 ①		MOSFET symbol
	(Body Diode)				А	showing the
I _{SM}	Pulsed Source Current			1544	~	integral reverse
	(Body Diode) ②					p-n junction diode.
V _{SD}	Diode Forward Voltage			1.3	V	$T_{J} = 25^{\circ}C, I_{S} = 195A, V_{GS} = 0V$ (5)
t _{rr}	Reverse Recovery Time		41	62		$T_J = 25^{\circ}C$ $V_R = 34V$,
			51	77	ns	$T_J = 125^{\circ}C$ $I_F = 232A$
Q _{rr}	Reverse Recovery Charge		62	93		T _J = 25°C di/dt = 100A/µs ⑤
			99	149	nC	T _J = 125°C
I _{RRM}	Reverse Recovery Current		2.3	-	Α	$T_J = 25^{\circ}C$
t _{on}	Forward Turn-On Time	Intrins	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)			

Notes:

 \odot Calculated continuous current based on maximum allowable junction $\textcircled{I}_{SD} \le 232A$, di/dt $\le 907A/\mu s$, $V_{DD} \le V_{(BR)DSS}$, $T_J \le 175^{\circ}C$. temperature. Package limitation current is 240A. Note that current limitations arising from heating of the device leads may occur with some lead mounting arrangements.(Refer to AN-1140

http://www.irf.com/technical-info/appnotes/an-1140.pdf

- 2 Repetitive rating; pulse width limited by max. junction temperature.
- 3 Limited by T_Jmax, starting T_J = 25°C, L = 0.018mH $R_G = 50\Omega$, $I_{AS} = 232A$, $V_{GS} = 10V$. Part not recommended for use above this value.
- (5) Pulse width \leq 400µs; duty cycle \leq 2%.
- $\ensuremath{\mathbb{G}}$ C_{oss} eff. (TR) is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- $\oslash\ C_{oss}$ eff. (ER) is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .
- R_{θ} is measured at T_J approximately 90°C.

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V_{GS}, Gate-to-Source Voltage (V)





Fig 5. Typical Capacitance vs. Drain-to-Source Voltage www.irf.com



Fig 2. Typical Output Characteristics



Fig 4. Normalized On-Resistance vs. Temperature



Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

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Fig 12. Maximum Avalanche Energy vs. DrainCurrent



Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case



Fig 14. Typical Avalanche Current vs. Pulsewidth



Fig 15. Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 14, 15: (For further info, see AN-1005 at www.irf.com)

- 1. Avalanche failures assumption: Purely a thermal phenomenon and failure occurs at a temperature far in
 - excess of T_{jmax} . This is validated for every part type.

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- 2. Safe operation in Avalanche is allowed as long asT_{jmax} is not exceeded.
- 3. Equation below based on circuit and waveforms shown in Figure 22a, 22b.
- 4. $P_{D (ave)}$ = Average power dissipation per single avalanche pulse.
- 5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
- 6. I_{av} = Allowable avalanche current.
- 7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
 - t_{av =} Average time in avalanche.

 $D = Duty cycle in avalanche = t_{av} \cdot f$

 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$\begin{split} \textbf{P}_{D \;(ave)} &= 1/2 \;(\; \textbf{1.3} \cdot \textbf{BV} \cdot \textbf{I}_{av}) = \Delta T/ \; \textbf{Z}_{thJC} \\ \textbf{I}_{av} &= 2 \Delta T/ \; [\textbf{1.3} \cdot \textbf{BV} \cdot \textbf{Z}_{th}] \\ \textbf{E}_{AS \;(AR)} &= \textbf{P}_{D \;(ave)} \cdot \textbf{t}_{av} \end{split}$$



Fig 16. Threshold Voltage vs. Temperature

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Fig 23a. Switching Time Test Circuit



Fig 24a. Gate Charge Test Circuit www.irf.com







Fig 23b. Switching Time Waveforms



Fig 24b. Gate Charge Waveform

TO-262 WideLead Package Outline

Dimensions are shown in millimeters (inches)





SEATING PLANE

Δ

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994

2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].

▲ DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.

4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.

5. DIMENSION 63, 65, 67, 69 AND c1 APPLY TO BASE METAL ONLY. 6. CONTROLLING DIMENSION: INCH.

7.- OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

LEAD ASSIGNMENTS

HEXFET 1.- GATE 2.- DRAIN 3.- SOURCE



TO-262 WideLead Part Marking Information



Lot Code

Ordering Information

Base part number	Package Type	Standard Pack	Complete Part Number	
		Form	Quantity	
AUIRF3004WL	TO-262 WideLead	Tube	50	AUIRF3004WL

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